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TASK III REPORT—LOW COST AIRBORNE MICROWAVE LANDING SYSTEM RECEIVER

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American Electronic Laboratories, Inc.

for

AMES RESEARCH CENTER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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INTRODUCTION

This document is the Task III report for the Low Cost Airborne Microwave Landing System (MLS) Receiver program, sponsored by NASA Ames Research Center, under contract NAS2-9332. This report summarizes all work performed under the contract, and summarizes the first, second, third, and fourth quarterly progress reports.

Included within this report is a detailed description of the prototype low cost MLS receiver developed under the contract. This detail includes block diagrams, schematics, board assembly drawings, photographs of subassemblies, mechanical construction, parts lists and microprocessor software, in addition to test procedures and results. This detailed information is considered sufficient to allow anyone skilled in the art to understand the receiver operation. However, it is not necessarily intended as sufficient information to allow direct manufacturing. Accordingly, neither NASA nor AEL nor NARCO accepts the responsibility for completeness or accuracy of final design details.

It is felt that this report contains sufficient information to allow a capable commercial avionics equipment manufacturer to analyze the complexity, operation, non-recurring and recurring costs associated with production of a general aviation MLS receiver. In all likelihood, a manufacturer would modify the design described herein in such a way as to utilize materials, parts and processes that represent the lowest manufacturing cost to him. Furthermore, certain design improvements will be made in later phases of this project.

The manufacturing costs analyzed in section 9 of this report represent the best estimates of NARCO and AEL, using their costing procedures, loadings, etc. Manufacturers contemplating the MLS market must apply their own cost factors. Again, the costs are presented as estimates; they are not guaranteed by NASA, AEL or NARCO.

Persons aiding the authors in the preparation of this report are, from AEL: F. Decker, N. Jespersen, R. Shillady, and J. Kryzanowsky. The contributors from NARCO were: D. Anderson, R. Powell and I. Stephen.

This effort was under the direction of Mr. J. Pope, COTR, NASA Ames Research Center, Moffett Field, California.

Summary of Program Accomplishments

AEL, together with their major subcontractor NARCO Avionics, has succeeded in designing and producing a Microwave Landing System receiver essentially suitable for general aviation. AEL has produced flyable, working receivers that are adequate for landing purposes. It is this operating receiver design that has been priced out as

saleable at a manufacturers suggested list price of $1485, installed in a general aviation aircraft. This result can be favorably compared to the original cost goal of $1250 in 1976 dollars.

The $1485 sell prices, when related to manufacturing cost, is achieved by a total loaded labor and material cost of $408, of which $243 is material, $55 is direct labor, and $111 is manufacturing overhead (200%). Accordingly it was obvious from the onset that the receiver must be consistent with high volume automated manufacturing, utilizing low cost commercial grade parts. AEL's task, on this design-to-price program, was to analyze, evaluate and implement optimum cost/performance tradeoffs such as to achieve a minimum projected receiver cost in production lots of 2000. In order to accomplish this, an orderly process of technique evaluation and control had to be implemented, as described in the following section.

Cost Versus Performance

From the beginning of this program, it was immediately apparent that a very large number of tradeoffs existed, with interdependency among tradeoffs being the general case and seldom the case whereby a simple cost versus performance choice could be made. Thus it was determined early in the program to utilize the candidate versus challenging alternate approach to the design-to-price effort. This technique is based on generation of a sound candidate approach meeting all specifications, and generation of alternate "challenges" to any portion of the candidate. Each alternate, when qualified, is priced out in detail. Figure 1 illustrates this process. In order for an alternate to qualify, it must be determined to:

1) Meet the applicable specifications of that portion of the receiver with occasional exceptions in areas that could be potentially relaxed.

2) Be compatible with available printed circuit area, volume and construction techniques.

3) Be almost obviously of lower cost in either raw material or production loaded labor.

4) Be of a technology that is compatible with general aviation equipment manufacturing engineering skills.

As a result, alternates which are cheaper but do not meet the specification, which are large and bulky, or which are advanced research items for military use generally do not qualify as viable alternates.

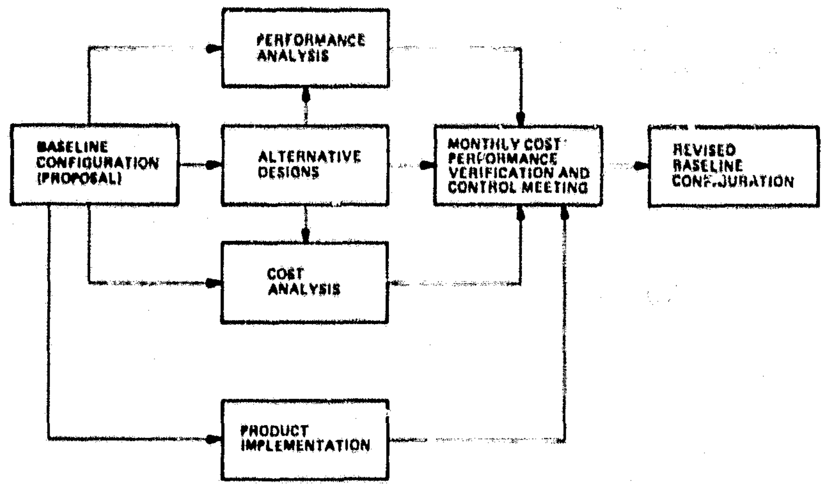

FIGURE 1. COST PERFORMANCE ALTERNATE EVALUATION AND CONTROL

However, each candidate receiver subassembly has several viable alternates. The SOW clearly and correctly pointed out the necessity of concentrating the contract resources on those "... MLS receiver subassemblies which represent the highest percentage of receiver cost hence, greatest potential for significant cost savings considering the appropriate cost/performance tradeoffs."

Accordingly, the areas discussed in the following three paragraphs received a heavily concentrated effort during the study phase of this program.

Microwave components. - It is apparent that the microwave portion of an item such as the MLS Receiver can be very expensive. C-band filters, mixers and local oscillators are ordinarily purchased by avionics equipment manufacturers on a competitive basis, but are nevertheless relatively expensive. As will be shown later, the purchase of conventional microwave components would double the $1250 cost goal. AEL, which has had extensive experience in microwave component design and fabrication, has shown that the technology for the low cost microwave front end must be custom stripline, which integrates the two precision filters and the mixer. The precision stripline filters, which would be prohibitively expensive in any other form, then allow a simple multiplier technique. The microwave (RF Head) area was the most intensely studied portion of the Technique Selection Study, and the justification is apparent. This area is described in meticulous detail in the Microwave RF Head Electronics portion of this report.

Log IF and demodulator. - One intrinsic characteristic of the TRSB system is the necessity of either a potentially complex logarithmic amplifier or a precision AGC able to provide a gain characteristic that is compatible with the envelope processor detection. The Bendix MLS Airborne Subsystem, Basic Configuration, for example, utilized a 6-stage successive approximation log IF that could contribute heavily to the receiver cost, being surpassed only by the microwave and microprocessor subassemblies.

AEL has extensively evaluated use of the commercial RCA CA3089 IF integrated circuit, which contains both a log IF and an FM demodulator suitable for the DPSK data detection, and has so far found it acceptable. The corresponding circuit reduction in material cost, alignment cost, size and complexity is very significant for this program. However, it must be admitted that this device, although the least expensive approach by far, does not provide the best achievable signal sensitivity. Accordingly, in later phases, other low cost but more elaborate log IF and DPSK detectors will be explored, in anticipation of possible future requirements for additional MLS receiver sensitivity.

Processor. - A third major area involves the processor. Specifically, it was determined early that a commercially available microprocessor was ideally suited for the MLS receiver. The concept of a dedicated LSI development was discarded due to the anticipated reluctance of the general aviation equipment manufacturer to accept the development cost and risks. Furthermore, it was determined early that microprocessors exist that provide adequate computing ability to handle the MLS requirement at moderate cost. Thus the problem was systematically reduced to that of choosing a microprocessor and memory having high enough throughput at minimum total cost. It was an early determination that several medium throughput, moderate price systems are available, thereby giving the equipment manufacturer some flexibility in choice, with a high probability of being compatible with his other general aviation equipment products.

RECEIVER SYSTEM APPROACH

The MLS receiver described herein is a panel mounted unit with a remote microwave RF head. The panel mounted configuration was chosen as being the lowest cost in comparison to a remote electronics package being controlled by a cockpit mounted control panel.

The remote RF head utilizes RF filters, a mixer, and a local oscillator microwave multiplier integrated into the antenna housing. This technique eliminates the necessity for a costly low noise preamplifier, that would be otherwise needed to overcome RF losses in the antenna cable.

The panel-mounted receiver includes an On/Off Ident volume control, glideslope select switch, and integral channel selection. This system is designed to operate on Signal Formats as described in FAA-ER-700-08A, dated 30 May 1975, Amendment 1, dated 22 August 1975, Specification Change No. 1, and to provide the functional requirements a. through f. described in NASA ARC Specification II, Section 4.

The receiver system described herein provides the proper ARINC-578 output drive levels to existing ILS displays as required by Paragraph 2.0 of the SOW. The course deviation indicator (CDI), therefore, is assumed to be an existing unit and not a part of the system description except as it affects electrical and performance interfaces.

The key LCLMS performance parameters are shown in Table 1.

Block Diagram and General System Description

A block diagram of the candidate Low Cost MLS receiving system is shown in Figure 2. The system is composed of two basic units: a remote mounting RF head, and a panel mounting receiver. Interconnections between these two units have been minimized by supplying DC power to the RF head via the LO coaxial cable. Within the panel mounting receiver, interconnections between subassemblies also have been minimized by grouping those elements requiring multiple interconnections within the same subassembly to facilitate assembly and servicing.

An RF signal is received at the antenna, which is contained within the remote mounting RF head. The first item in the signal path is the RF preselector filter, realized in stripline, which provides immunity to spurious and image responses and provides added protection against LO radiation. Following this is the first mixer, also fabricated in stripline, followed by the first IF preamplifier. Also contained in the RF head are the X16 LO multiplier and the LO bandpass filter. The preselector, mixer, and LO filter are stripline structures. The major components relating to receiver sensitivity are thus intimately located at the antenna for the purpose of minimizing losses.

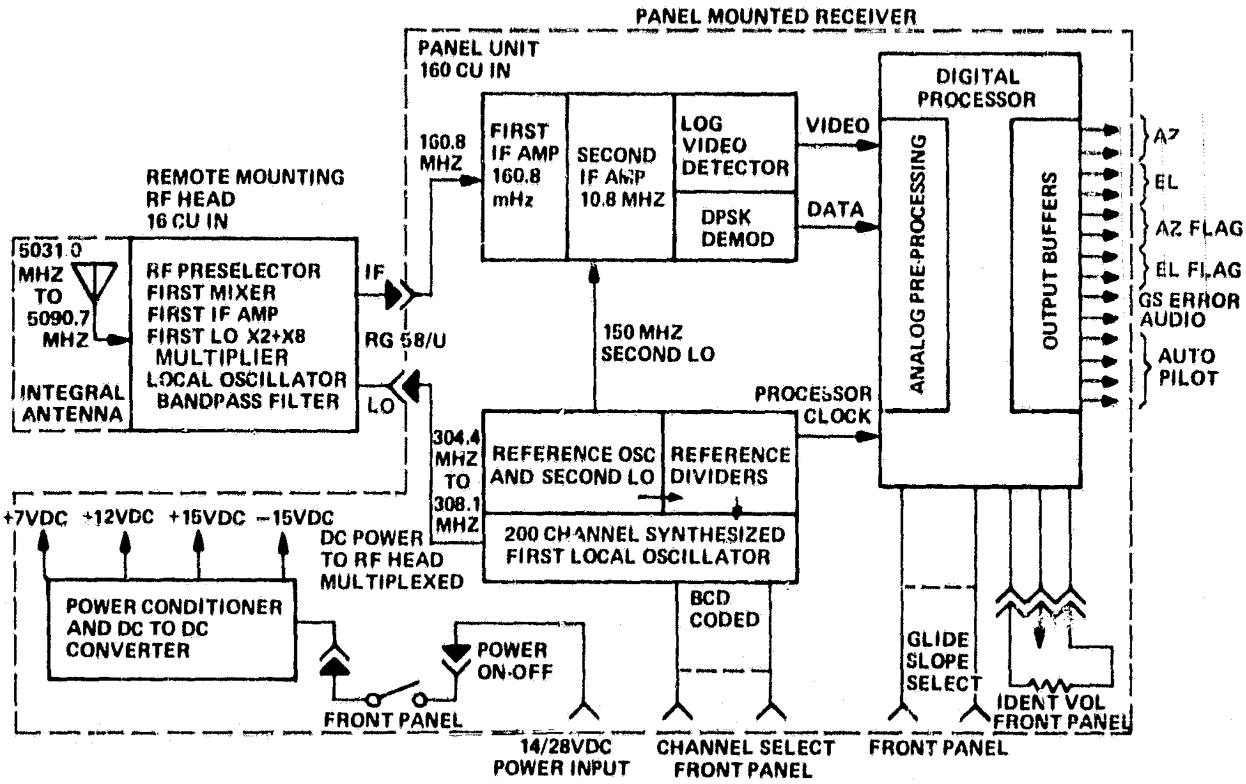

FIGURE 2. LOW COST MLS RECEIVER BLOCK DIAGRAM

The IF output of the RF head is routed to the panel mounting receiver unit, wherein it is first applied to the 160.8 MHz IF amplifier in the IF/detector subassembly. This is followed by conversion to the second IF frequency, logarithmic detection, and DPSK demodulation. The video and data outputs of the IF/detector module are applied to the processor module. The video is routed to the analog preprocessor section, which utilizes an adaptive threshold detector with outputs to the digital portion of the processor. The DPSK data, which at this point is in the form of amplitude transients representing phase transitions, is converted into one-zero data and outputted to the digital processor and is also used to synchronize a data clock utilized for data decoding.

The digital processor, the heart of which is a low cost microprocessor, decodes the DPSK data to determine facility identification, function, minimum glideslope, and ground status. In addition, it performs calculations based on the input video to determine angle data which is then smoothed digitally before being converted to analog signals and outputted to the ILS display and autopilot. Both flag signals and Morse code identification tones are generated in the digital processor. The pilot selectable glideslope information is applied to the digital processor. The remaining input to the processor is the clock, generated by the synthesizer.

The first local oscillator (LO) consists of a 200-channel phase-locked loop (PLL) frequency synthesizer. Synthesizer tuning information is received from the front panel switches. The first LO output is a 0 dBm signal in the frequency range of 304.4 MHz to 308.2 MHz. This synthesized LO signal is then sent to the remote mounted RF head where the signal frequency is multiplied by 16 to arrive at the final LO frequency. Required DC power for the remote head is sent over the same cable as the first LO signal. It is important that the LO frequency sent to the RF head is sufficiently removed from the 160.8 MHz first IF frequency so that the first IF filter can prevent this undesired component from reaching the second mixer.

Within the synthesizer subassembly is a 4.8 MHz crystal controlled reference oscillator which serves 3 functions: the 150 MHz second LO and the offset frequency for the first LO are derived from a fixed tuned oscillator phase locked to the reference; a 9.375 kHz Signal is derived and used as the reference clock for the 200 channel synthesizer; and a 1.6 MHz signal is derived for use as a data processing clock. This technique provides phase coherence of all internally generated signals with the exception of the 15 kHz data clock, which is by necessity phase-locked to the DPSK data.

The remaining subassembly in the receiver unit is the DC to DC converter and power conditioner. This switching type supply will accept either the 14 VDC or the 28 VDC input from the aircraft and, with a minimum efficiency of 80 percent, convert it to the seven voltages required by the system circuits. The +7 VDC output is locally regulated to +5 VDC at points of usage (primarily digital circuits) to provide improved regulation and isolation of these supply lines. The isolation of digital logic supply lines in this manner greatly reduces internal RFI due to required bundling of supply and control lines between subassemblies.

A photograph of the MLS receiver, showing both the panel mounted unit and the RF head, is shown in Figure 3.

Noise Figure and Sensitivity

The receiver noise figure is an important parameter in relationship to receiver sensitivity. Since the low cost design precludes the possibility of a low noise 5 GHz GaAs FET amplifier, it is essential that the losses prior to the first active amplifier stage be kept to a minimum.

The losses to be minimized are those associated with the RF preselector filter and the first mixer. The RF preselector loss is related to the RF selectivity, which in turn relates to the parameters of interference rejection, image rejection, and LO reradiation rejection. Mixer loss relates to LO drive level and bias, which also relates to signal handling capability and intermodulation product rejection. Further tradeoff considerations are discussed in Microwave RF Head Electronics portion of this report.

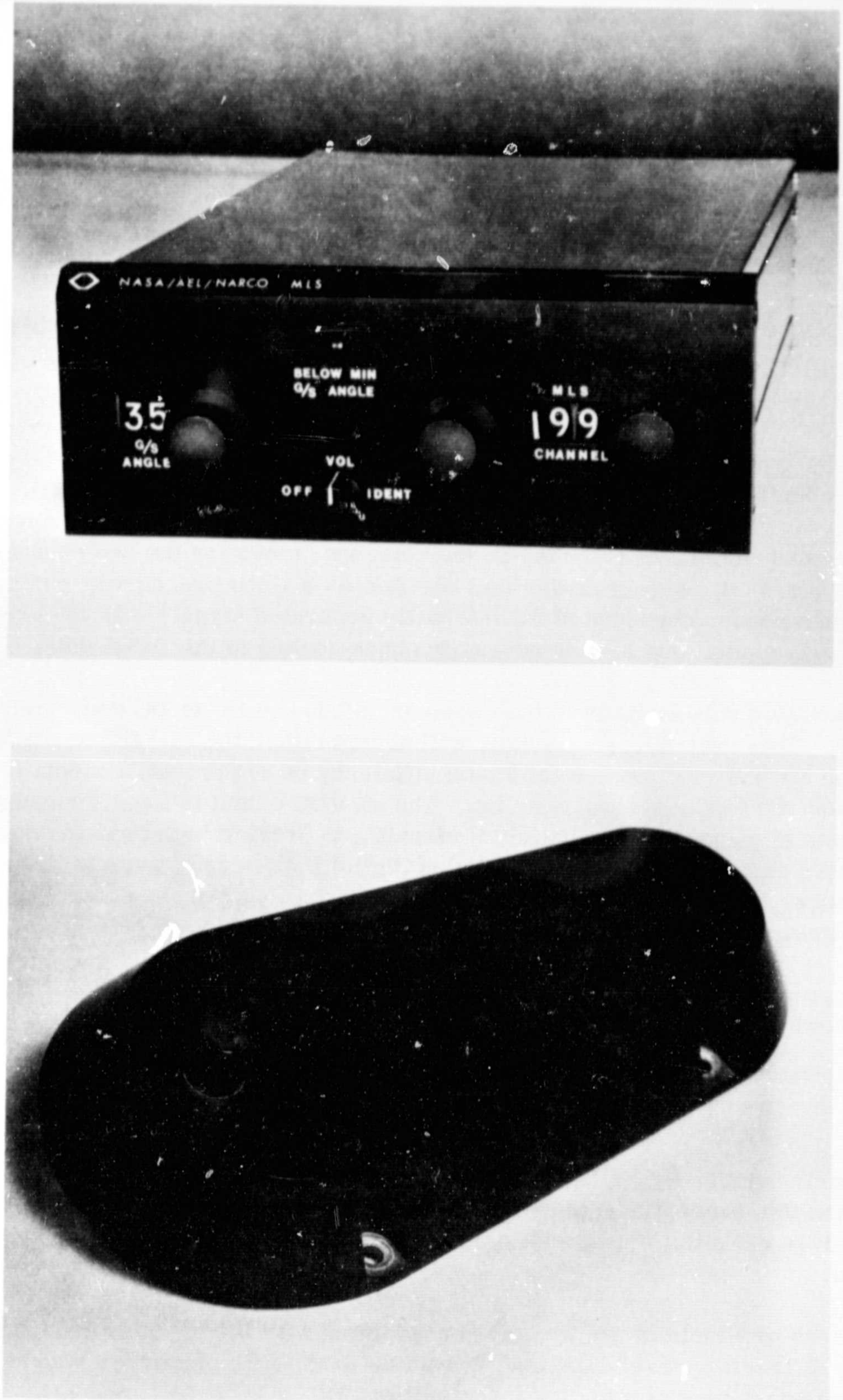

FIGURE 3. MLS PANEL MOUNTED UNIT AND REMOTE RF. HEAD

The nominal noise figure and gain calculations are shown in Figure 4. The stage parameters of noise figure and gain are shown above each block and the calculated composite noise figure, cumulative gain and minimum signal levels are listed below. The -96 dBm sensitivity level is based on a 10 dB signal to noise level in a 225 kHz IF bandwidth.

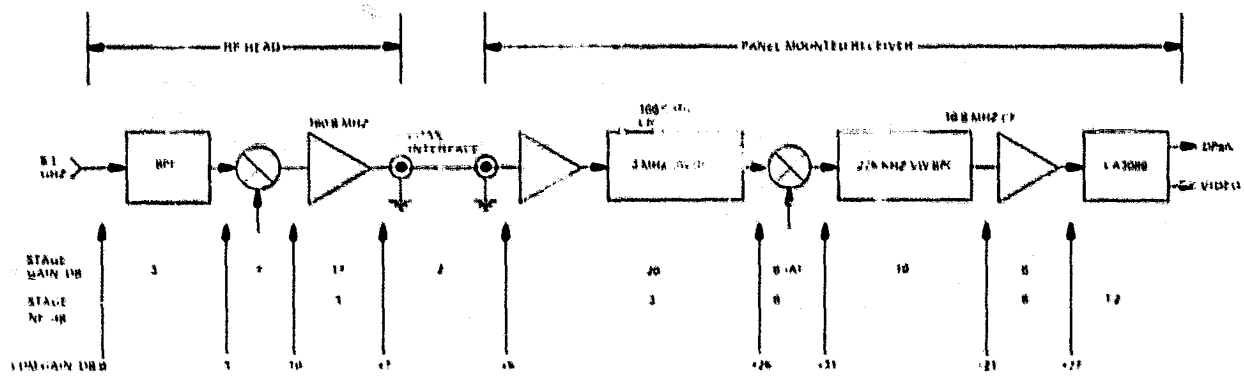

FIGURE 4. NOISE FIGURE AND GAIN ANALYSIS

TABLE 1. SALIENT LCMLS PERFORMANCE PARAMETERS

	SPECIFICATION GOAL	ACTUAL
OPERATING FREQUENCY	5031.0 - 5090.7	Same
NO. OF CHANNELS	200	Same
CHANNEL SPACING	300 KHz	Same
SIGNAL FORMAT	FAA-ER-800-08A	Same
IMAGE REJECTION (PRIMARY)	60 dB	40 dB
IMAGE REJECTION (SECONDARY)	60 dB	60 dB
NOISE FIGURE	NS	14 dB
IF BANDWIDTH	150 KHz min	225 KHz
ADJACENT CHANNEL (REJECTION INTERFERENCE)	50 dB	40 dB
TANGENTIAL SENSITIVITY DPSK	-98 dBm	-90 dBm
AZIMUTH SCALE FACTOR	± 2.5° FS	Same
ELEVATION SCALE FACTOR	± 0.7° FS	Same
GLIDE SLOPE SELECTION	2.5-8°, 0.5° steps	Same
ANTENNA POLARIZATION	Vertical	Same
ANTENNA GAIN, HORIZONTAL	-3dbi, omni	0dbi ±60°
ANTENNA GAIN, VERTICAL	-3dbi, +25°, -30°	0dbi, +45°, -15°
POWER	14 watts	1 Ampere max, 12-28 VDC
WEIGHT	6.5 lb.	6.0 lbs.

MICROWAVE RF HEAD ELECTRONICS

This section describes the antenna, microwave filters and mixer, microwave LO multiplier, and RF head packaging.

The primary consideration in the remoting of the RF head is the elimination of a long, bulky, and expensive low loss cable at the MLS system frequency. The integration of the RF head and the antenna, which is an extension of the RF stripline structure, is a natural step and is described in this section. In this system, only two coaxial cables are required to service the remote antenna/RF head. These cables carry nominally 306 and 160 MHz respectively, and may be a standard type such as RG-58 of which most installers are familiar. The installation of this 5 GHz MLS system is therefore no more complex or risky than the installation of a current NAV system. By remote mounting (close to or integral with the antenna) the RF head, the antenna cable losses can be minimized such that allowable system noise figures can be achieved without the use of expensive 5 GHz preamplifiers.

Antenna Cost/Performance Trade-Offs

A number of different types of antenna were considered as candidates for the low cost MLS antenna. Table 2 lists these types and the performance/cost trade-offs. The project goal is a low cost antenna which meets the pattern and gain requirements previously described in Table 1. The cost of the antenna is determined by two factors: the cost of the antenna element, and the cost of the RF stripline antenna interface. Another cost factor is the DC grounding of the antenna for lightning protection. If the antenna element is not DC-grounded, lightning protection must be added to the RF circuitry at added cost.

After reviewing the above factors, the list of candidates in Table 2 was reduced to the last four types listed. It was decided not to continue the dipole investigation, since similar results could be obtained with a monopole, which is easier to feed by the stripline. The remaining three types of antennas were thoroughly investigated. All three provide a good impedance match over the required bandwidth. The radiation pattern shape is more dependent on the shape of the ground plane than on the element type. The "hair pin" antenna was selected as the best overall element. Its cost is less than the microstrip cone and is about the same as a simple monopole, and the "hair pin" element is DC grounded. The element is low cost, easily produced and meets the requirements of the MLS system.

TABLE 2. ANTENNA DESIGN TRADE-OFFS

Antenna Type	Relative Cost	Omni Pattern for ± 90°	Aerodynamic Size	Weight	Ease of Stripline Feed	DC Grounded
1. Rectangular Horn	High	No	Large	Moderate	Difficult	Yes
2. Biconical Horn	High	Yes	Large	Moderate	Moderate	No
3. Co-Linear Array	High	Yes	Small	Low	Difficult	No
4. MIC Element	Low	Yes	Moderate	Low	Moderate	No
5. Slot	Low	No	Small	Low	Simple	Yes
6. Dipole	Low	Yes	Small	Low	Moderate	No
7. Microstrip Cone	Low	Yes	Small	Low	Moderate	Yes
8. Monopole	Very Low	Yes	Small	Low	Simple	No
9. Hair Pin	Very Low	Yes	Small	Low	Simple	Yes

The "hair pin" performance was optimized by adjusting the shape of the hair pin and its position on the RF substrate. A monopole with various shorting sections was tested. The "h" type element shown in Figure 5 gave the best results.

Antenna performance. - This antenna is designed to operate on either metal or non-metallic mounting surfaces, without the added cost of an additional metal ground plate. The VSWR of the antenna, shown in Figure 6, is less than 1.75:1 from 5.0 GHz to 5.1 GHz, relatively independent of the type of mounting surface. The following performance discussion applies to an antenna mounted on a non-metallic surface.

The brassboard antenna pattern was within the required 3 dB of omnidirectional in the horizontal plane for angles within ± 120 degrees of the nose of the aircraft, as shown in Figure 7. The gain was greater than 3 dB above an isotropic radiator at the horizon. The approximate 6 dB front-to-back ratio is caused by the asymmetric mounting and the back "leg" of the antenna element. This ratio increases the number of available mounting locations, because any interference caused by items behind the antenna (i.e., vertical stabilizers, loading gear, etc.) is reduced. The 3 dB points in the elevation plane for the forward hemisphere are greater than the required +25 and -30 degrees from the horizon, as shown in Figure 8. The reception of horizontally polarized signals is 10 dB below the vertical signal for any horizontal direction in the front hemisphere. The antenna's pattern performance lends itself to either top or bottom aircraft mounting.

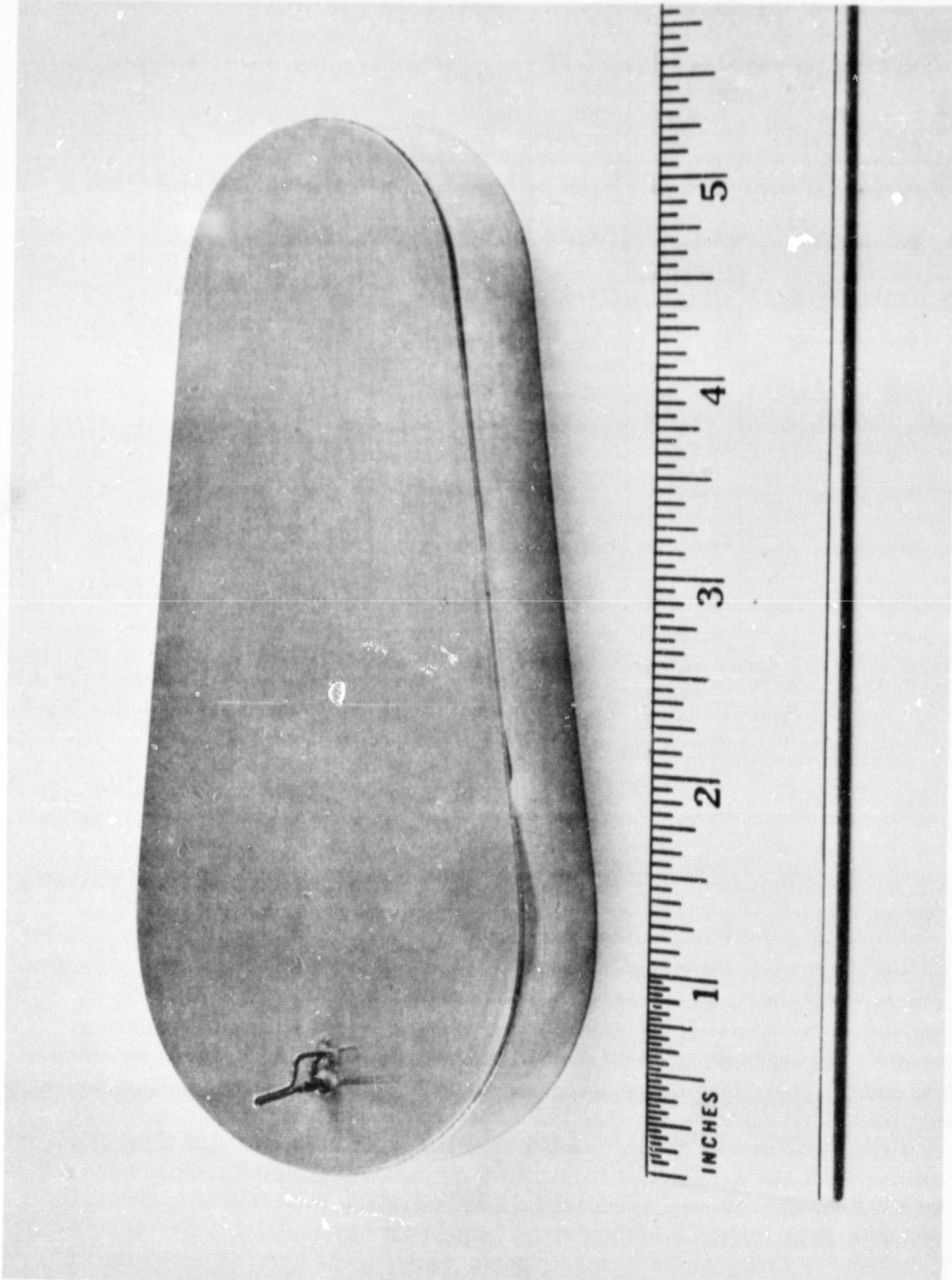

FIGURE 5. "H" ANTENNA TYPE

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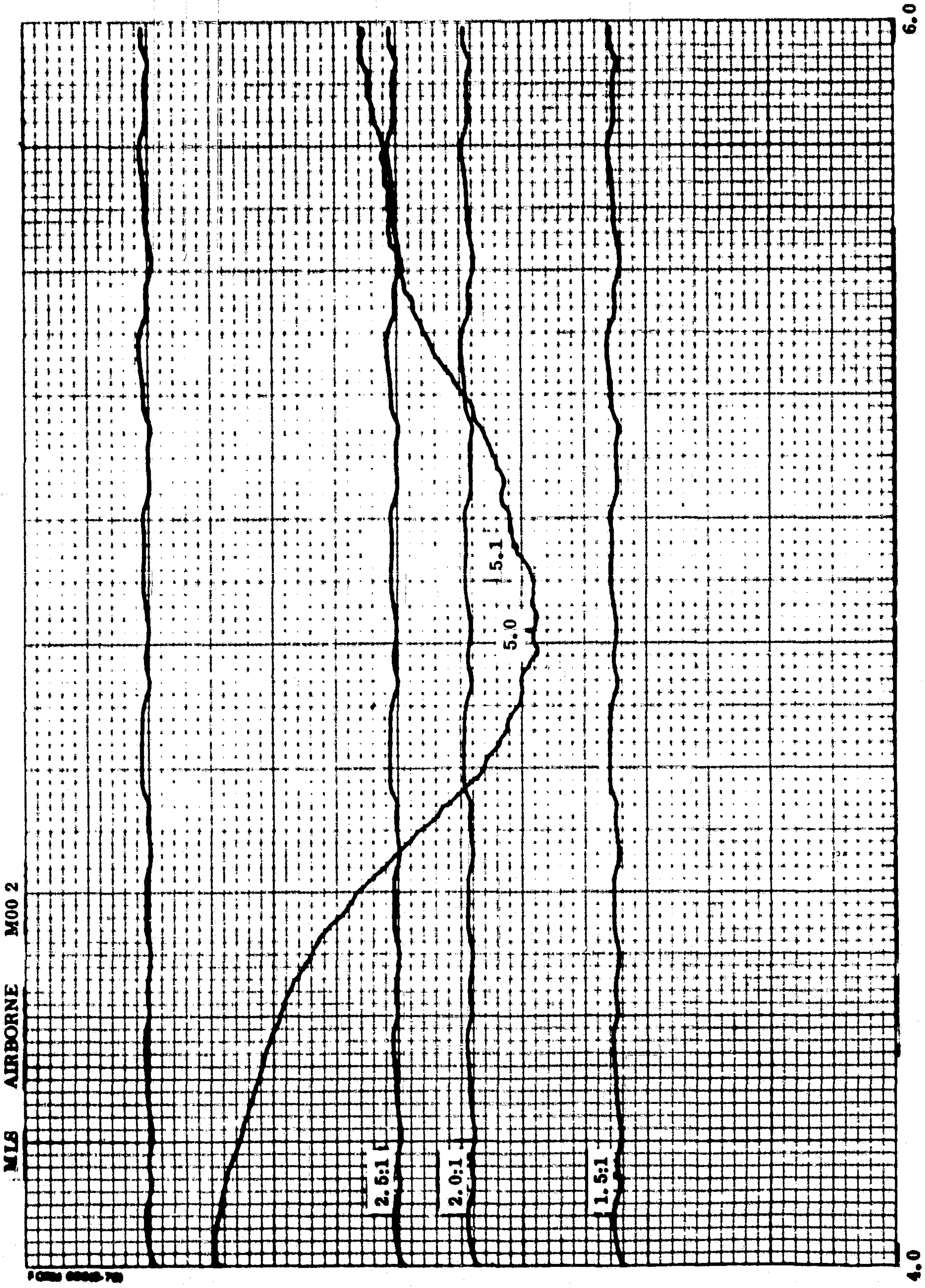

FIGURE 6. MLS BRASSBOARD ANTENNA MODEL VSWR

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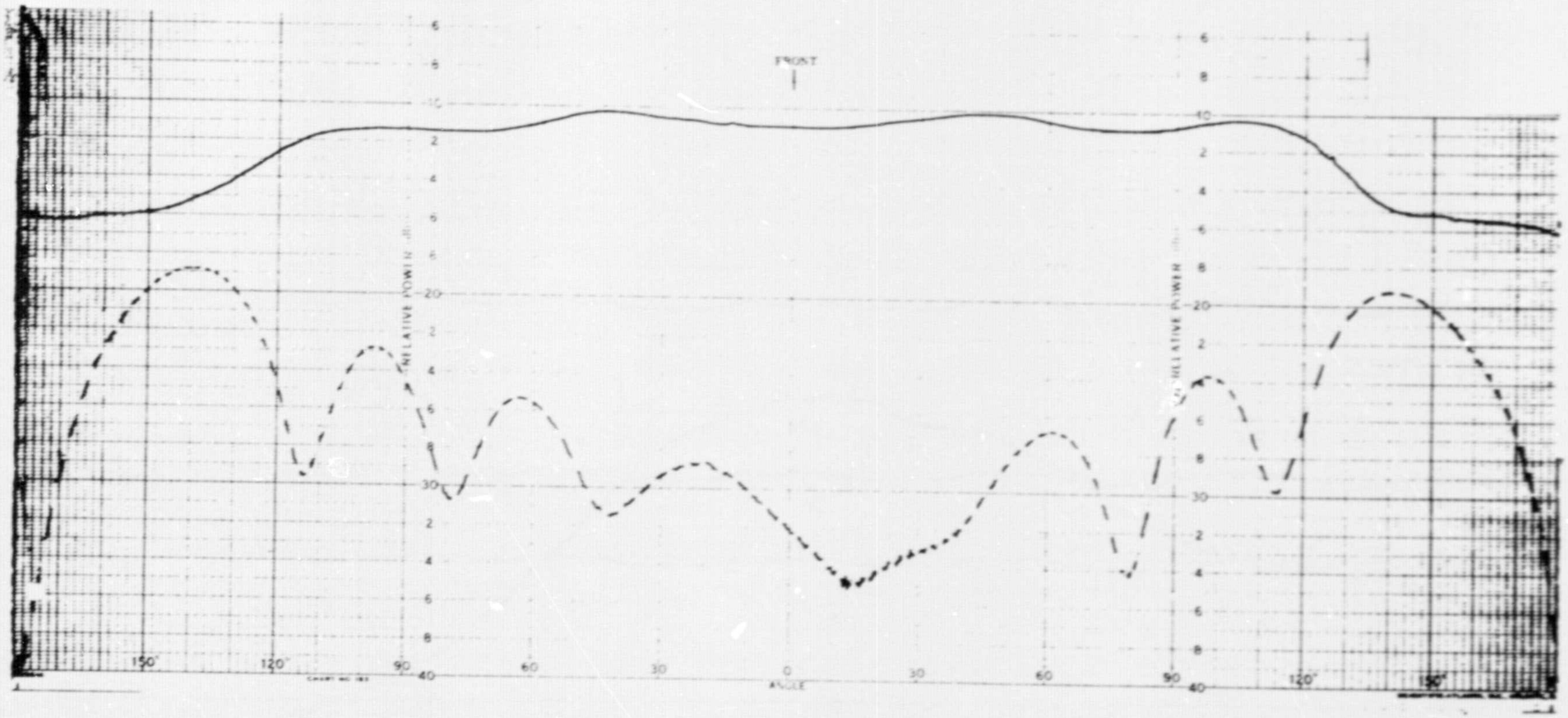

FIGURE 7. MLS BRASSBOARD ANTENNA AZIMUTH AT ZERO DEGREES ELEVATION

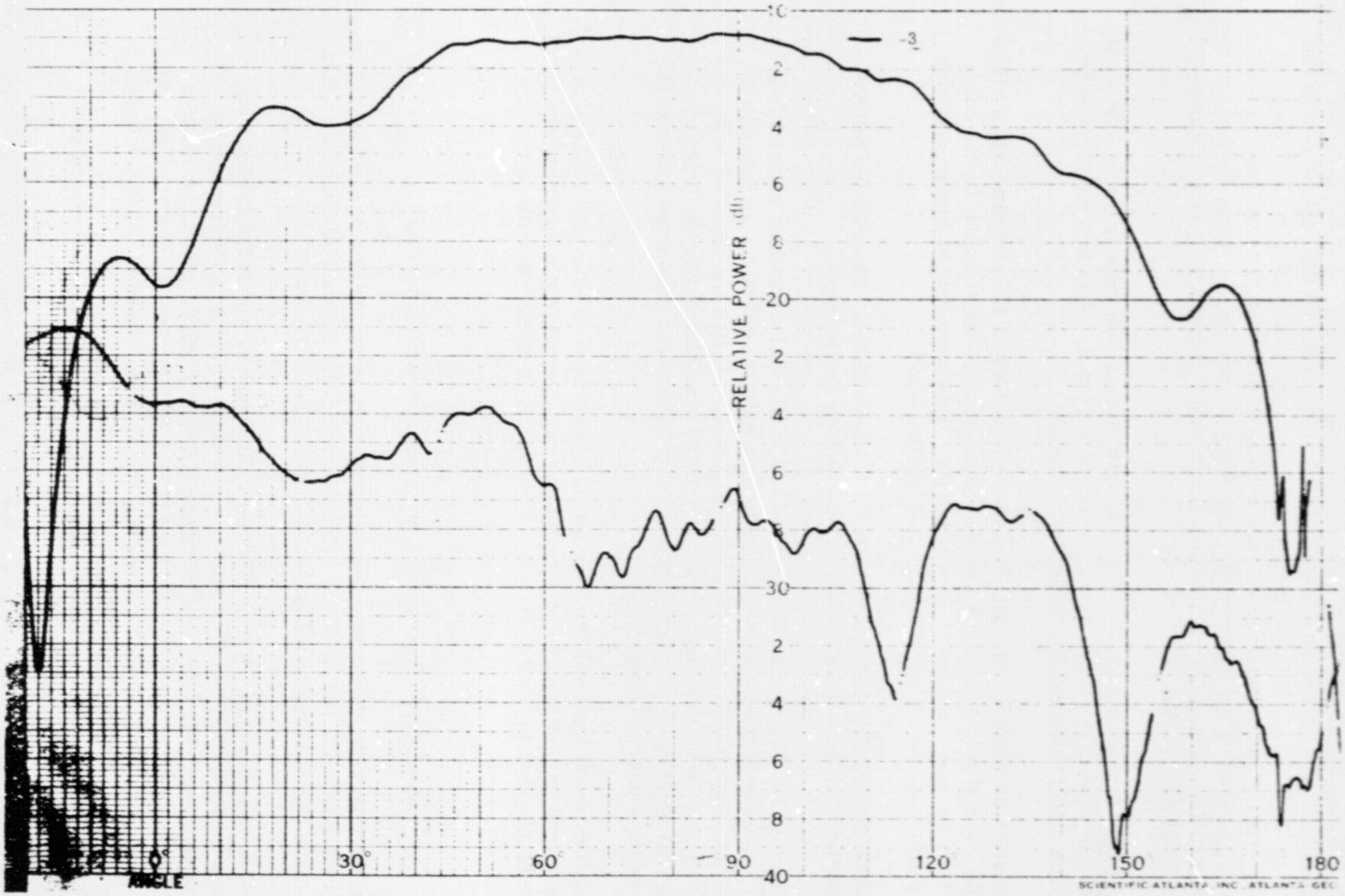

FIGURE 8. MLS BRASSBOARD ANTENNA ELEVATION

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When the antenna is placed on a metal ground plane, such as the cockpit roof of the Cessna 402 or DeHavilland DHC-6, the elevation patterns will tend to cut off closer to the horizon. This effect is minimized if the antenna is mounted near the front of the surface or is mounted on a surface with a slight nose-down slope. When the antenna is mounted on a metal surface the reception of horizontally polarized signals is reduced by about an additional 10 dB.

Mechanical construction. - The "hair pin" antenna element is formed by bending a section of #20 wire to the shape as was shown in Figure 5. This is a rugged antenna element which easily interfaces with the RF stripline.

The antenna element is connected to the input port of RF stripline via a stripline feedthrough. The ground lead of the element feeds through the stripline layers connecting to both the upper and lower ground planes. This assembly technique provides both good electrical contact and a rugged mechanical mount.

The entire antenna/RF unit is encased in a plastic radome. The radome mechanically strengthens the antenna and protects it from the environment.

Mounting. - The antenna is designed to operate with or without a metallic ground plane. Its radiation patterns will provide adequate gain for either top or bottom aircraft mounting. Acceptable performance will be obtained, in a top mounted case, for surfaces from 0 to 30 degrees nose down. On metal mounting surfaces, it is recommended that the antenna be mounted approximately 15 degrees nose down and near the front edge of the surface, if possible.

The small size and light weight of the antenna permits it to be mounted on any aircraft surface with minimum structural modification. The antenna's front-to-back ratio allows it to be mounted in front of structural members or other antennas on the aircraft.

Microwave Electronics Cost/Performance Trade-Offs

Several transmission media are currently available which may be contemplated for use in the construction of the RF head. The electrical and mechanical characteristics of each of these are considered below.

Waveguide supports both TM and TE propagation modes, and is the lowest loss transmission media available. Waveguide is mechanically rigid and structurally strong; however, design in this medium results in a very bulky system. A relative size may be obtained by considering the length of a quarter wave in this medium. At 5 GHz in waveguide, $\frac{\lambda}{4} = 0.57$ inch, which implies an overall size of about 8.5 inches by 4 inches by 3 inches. Machining and assembly is expensive, since precision welding and metal work is required.

Coax propagates energy in a TEM mode and can be a low loss material, dependent upon the dielectric used in construction. Coax also gives rise to a mechanically rigid assembly, but it is bulky ($\frac{\lambda}{4}$ = 0.41 inch at 5 GHz in coax implying an overall size of about 6 inches by 3 inches by 3 inches). Machining and assembly is expensive, since precision parts are required.

Microstrip is generally constructed on alumina substrates and propagates a quasi-TEM mode (> 99.5% pure Al_2O_3). This medium is a low-to-medium-loss material, but it is extremely brittle (glass-like) and expensive. Of the materials considered, alumina yields the smallest size ($\frac{\lambda}{4}$ = 0.19 inch at 5 GHz, yielding an overall size of about 2.8 inches by 1.3 inches by 0.2 inch). Machining and assembly is minimal, since lithographic techniques can be employed.

Air line construction utilizes what the literature calls suspended substrate stripline techniques. The transmission media is formed when a Kapton (or other similar material) substrate with the circuitry etched onto it is suspended between two ground planes. An air channel is formed around the printed transmission line. The transmission mode is TEM and the Kapton/air combination is low loss, flexible and inexpensive. With a quarter wavelength about the same as in waveguide ($\frac{\lambda}{4}$ = 0.57 inch), the construction is somewhat bulky, with the thickness being about 1.5 inches as opposed to 3 inches in waveguide. Assembly time is minimal; however, tooling cost for setting up the stamping dies (for forming the groundplane channels) is very expensive. This construction may be sensitive to severe vibration. If the Kapton substrate resonates mechanically in the channel, fracture may occur. Severe mistuning of the printed board is also a possibility. Wide temperature variation may have a detrimental affect on the circuitry.

Stripline is also a TEM mode transmission medium. Stripline is constructed by sandwiching copper conductors between dielectric sheets metallized on the outer surface to form a ground plane. The structure is low-to-medium-loss, depending upon the dielectric material. The structure is flexible, yet it can be mounted in a manner not adversely affected by vibration. Stripline yields a medium-sized circuit as part of the RF head ($\frac{\lambda}{4}$ = 0.37 inch yields a package size about 5.4 inches by 2.5 inches by 0.6 inch). Machining and assembly costs are minimal, since stripline parts are constructed using photolithographic techniques.

Choice of transmission medium. - From the general description above, the indication is that stripline affords the best cost/performance tradeoff. A more detailed characterization of stripline follows, including an analysis of various stripline materials. See Figure 9 for a summary.

WAVEGUIDE:

* VERY LOW LOSS, RIGID, MECHANICALLY SOUND
* BULKY; $\lambda/4$ @ 5 GHz $\approx$ 0.57"
* MACHINING & ASSEMBLY EXPENSIVE

COAX:

* LOW LOSS MATERIAL, RIGID, MECHANICALLY SOUND
* BULKY; $\lambda/4$ @ 5 GHz $\approx$ 0.41"
* MACHINING & ASSEMBLY EXPENSIVE

MICROSTRIP:

* LOW TO MEDIUM LOSS MATERIAL (ALUMINA), BRITTLE (LIKE GLASS), EXPENSIVE
* SMALL SIZE; $\lambda/4$ @ 5 GHz $\approx$ 0.19"
* MACHINING & ASSEMBLY MINIMAL

AIR LINE:

* LOW LOSS MATERIAL (KAPTON), FLEXIBLE, INEXPENSIVE
* SOMEWHAT BULKY; $\lambda/4$ @ 5 GHz $\approx$ 0.57"
* TOOLING COST HIGH, MINIMAL ASSEMBLY TIME
* MAY BE SENSITIVE TO SEVERE VIBRATION

COPLANAR WAVEGUIDE, SLOT LINE: (SAME AS MICROSTRIP)

STRIPLINE:

* LOW TO MEDIUM LOSS MATERIAL (TEFLON-GLASS), FLEXIBLE, MEDIUM EXPENSE
* MEDIUM SIZE; $\lambda/4$ @ 5 GHz $\approx$ 0.37"
* MACHINING & ASSEMBLY COST MINIMAL

FIGURE 9. RF HEAD IMPLEMENTATION MEDIA

Polyphenelene Oxide (PPO) is a low-to-medium-loss material. It has good flexibility and negligible cold flow characteristics, but if placed under any kind of stress at all, it manifests stress crazing. The problem arises with time and temperature cycling. Also, PPO can not be punched or sheared, and it works best below 5 GHz. For these reasons, although it is an inexpensive material, PPO was deemed unacceptable for use in the RF head.

Epoxy-glass (G-10) is a high-loss material which performs best below 1 GHz. It has negligible to no cold flow characteristics and is easily punched or sheared. It has good flexibility and has negligible change in its properties with time or temperature cycling. Epoxy-glass is very inexpensive, but its lossy nature makes it unacceptable.

Glass reinforced polystyrene is a low-to-medium-loss material. It has poor flexibility and will break quite easily even in the glass reinforced variety. The time and temperature characteristics of this material are very poor, and it may not be punched or sheared. It has negligible to no cold flow, is quite useful at 5 GHz, and is an inexpensive material, but its mechanical properties make it unacceptable.

Polyolefin is a low loss material which is similar in appearance to polyethylene. It has good to fair time and temperature characteristics, and may be punched or sheared. Along with its excellent flexibility, polyolefin is subject to cold flow and severe warping when metallization is removed from one side. Polyolefin is a relatively inexpensive material, but its mechanical properties are unacceptable.

Teflon-glass is a low-to-medium-loss material with good flexibility and slight to negligible cold flow. It does not change much with time and has a wide working temperature range (-100 to +400 degrees Fahrenheit). It may be punched or sheared without problems, and it is excellent for use at 5 GHz and above. An appropriate choice of material is 3M type K-6098-GT which is 0.031 inch thick. The pricing of this material in a 2000 piece quantity yields a stripline package cost of about $5.56 per RF head.

Material choice. - Considerations from the previous paragraphs resulted in the selection of teflon-glass material for the stripline (See Figure 10 for a summary). Teflon-glass also lends itself to bonding; i.e., the two stripline plates are attached to one another under heat and pressure. Attaching subsequent components (mixer diodes, antenna and stripline connections) can be easily accomplished by a cut-and-plug operation.

Reliability. - The least reliable parts in the stripline package are the mixer diodes. The most likely causes for diode failure would be:

- Overvoltage on the bias line.
- Excessive LO drive.
- Excessive RF power.

POLYPHENELENE OXIDE (PPO)

* LOW TO MEDIUM LOSS MATERIAL
* GOOD FLEXIBILITY, BUT STRONGLY SUBJECT TO STRESS CRAZING WITH TIME AND TEMPERATURE CYCLING
* MAY NOT BE PUNCHED OR SHEARED
* WORKS BEST BELOW 5 GHZ
* NEGLIGIBLE COLD FLOW
* MEDIUM COST

EPOXY GLASS (G-10)

* HIGH LOSS MATERIAL
* NEGLIGIBLE TO NO COLD FLOW
* GOOD FLEXIBILITY, TIME AND TEMPERATURE CHARACTERISTICS
* MAY BE PUNCHED OR SHEARED
* WORKS BEST BELOW 1 GHZ
* VERY LOW COST

GLASS REINFORCED POLYSTYRENE

* LOW TO MEDIUM LOSS MATERIAL
* POOR FLEXIBILITY AND VERY POOR TIME AND TEMPERATURE CHARACTERISTICS
* NEGLIGIBLE TO NO COLD FLOW
* MAY NOT BE PUNCHED OR SHEARED
* USEFUL AT 5 GHZ
* LOW COST

TEFLON GLASS

* LOW TO MEDIUM LOSS MATERIAL
* GOOD FLEXIBILITY, TIME AND TEMPERATURE CHARACTERISTICS
* SLIGHT TO NEGLIGIBLE COLD FLOW
* MAY BE PUNCHED OR SHEARED
* EXCELLENT FOR USE AT 5 GHZ
* WILL BE BONDED TO FORM A SINGLE UNIT
* LOW COST

FIGURE 10. STRIPLINE MATERIAL CONSIDERATIONS

A typical burn-out level for mixer diodes is +30 dBm, CW, either at the RF or LO ports. Since LO drive is constant (around 0 dBm) and diode bias is controlled, excessive RF is likely to be the cause for diode burn-out; i.e., exposure of the RF head to high field strengths in the frequency range of the passband of the input circuitry.

The stripline package is mounted in a manner to prevent it from being subjected to mechanical strain. Failure in the stripline package, aside from diode failure, would likely entail the discarding of the entire RF head, since replacement of this unit would probably be less expensive than repair.

Interface with other components. - The stripline package interfaces with the following components:

- X16 Multiplier.
- Antenna.
- Test signal injection cable.
- IF Amplifier.
- Bias source for the mixer diodes.

The following stripline interfaces are established:

ITEM 1. The X16 multiplier is mounted on a board beneath the stripline. A section of transmission line feeds directly into the stripline at that point. A soldering operation is required.

ITEM 2. The antenna is soldered to the stripline through a hole in the upper ground plane. The other end of the antenna is soldered to the upper ground plane surface.

ITEM 3. The test signal is inserted into the stripline via a cable from a connector on the mounting surface of the RF head. A soldering operation is required.

ITEM 4. The first stage of the IF amplifier chain is located below the stripline on the same level as the X16 multiplier. Interface is via a piece of transmission line soldered to the stripline.

ITEM 5. A DC bias connection is required for the mixer diodes. A stranded wire serves this purpose.

Cost performance tradeoffs. - Some of the more significant cost performance tradeoffs are summarized below:

- A typical stripline material, K-6098 GT has a low relative dielectric constant (ϵ_r = 2.55) which results in a larger package than if alumina (ϵ_r = 10) were used. However, alumina is many times more expensive than K-6098, and is more difficult to process.
- Stripline requires two pieces of material as opposed to one in microstrip. Parts (such as diodes) are more difficult to interface with stripline circuitry.
- A 1/16-inch ground plane spacing results in somewhat loss loss than the proposed 1/32-inch spacing, but the overall circuit becomes larger in width by an approximate factor of two. Saving of material results from the choice of the thinner material.
- K-6098, although more costly than other stripline materials, is flexible, and is less likely to fracture under stress or severe vibration as compared to other materials considered.
- Another material, of slightly higher expense but more stable properties is Rogers Duroid 5880, with ϵ_r of 2.2 ± 0.04, offering tighter control in production.

Amplifier and Multiplier

The amplifier/multiplier section of the RF Head performs the function of amplifying and multiplying the 0 dBm, 304.8 to 308.1 MHz local oscillator input signal to a +7 dBm, 4876.8 to 4929.6 MHz mixer drive signal. Figures 11 and 12 show block diagrams of two configurations which were considered to accomplish this function. The block diagram shown in Figure 11 consists of two stages of lumped-element Class C amplifiers, which provide 23 dB of gain at the LO input frequency, followed by a distributed X16 multiplier with 16 dB conversion loss, which provides the required mixer drive signal. Figure 12 consists of a single stage amplifier, followed by an amplifier doubler which drives an octupler multiplier. In the following paragraphs, a discussion of a cost-effective amplifier design is begun, after which consideration is given to alternatives in achieving the required X16 multiplication. The circuit shown in Figure 12 is discussed in the multiplier section of this report.

Amplifier design. - The amplifier must provide enough multiplier drive to obtain a mixer LO drive level of about +7 dBm. By biasing the mixer, the drive level requirement could be reduced to as low as - 7 dBm, thereby eliminating the need for one of the two stages and resulting in a significant cost saving. For the purpose of this discussion, the two-stage amplifier-multiplier is described, since it provides higher output for better mixer performance. Multiplier conversion loss would be sacrificed in order to further simplify the multiplier design by providing

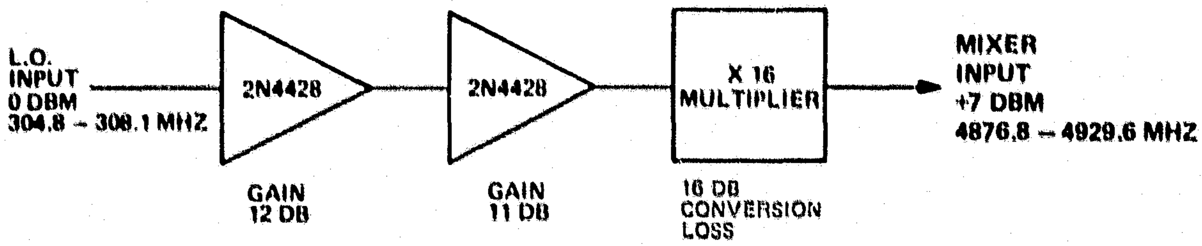

FIGURE 11. AMPLIFIER/MULTIPLIER USING X16 MULTIPLIER

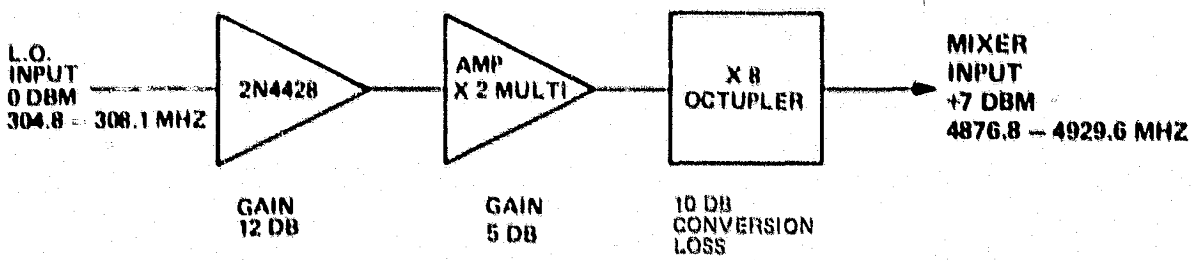

FIGURE 12. AMPLIFIER/MULTIPLIER USING X2 AMPLIFIER MULTIPLIER AND X8 OCTUPLER

lower level output. The multiplier is much more complex and costly than the amplifiers, therefore, if necessary, greater savings could be obtained by sacrificing performance in the multiplier.

The amplifier design is accomplished by using low Q matching circuits to maximize amplifier bandwidth so that minimum or no tuning is required after assembly. Low Q matching circuits also provide more stable circuit operation over the system's temperature range. Since the amplifiers are operated under Class C conditions, the transistor's input and output impedances are non-linear.

Multiplier design. - Several considerations must be made when choosing a X16 multiplier which will give maximum performance at minimum cost for the MLS receiver. Figure 13 shows a block diagram of three basic design techniques which will give X16 multiplication. Obviously, the multiplication could be achieved by using three of four stages of multiplication, but these concepts have been disregarded because of cost, assembly time, and tuning time. The blocks representing the individual multipliers can be designed using any element that has a non-linear output voltage versus linear input voltage characteristic. Three basic devices will be discussed in the following paragraphs with a brief description of device operation in the multiplying mode. Each device will be considered in a multiplier with a discussion of circuit simplicity, conversion efficiency, stability and cost. The three types of devices are varactor diodes, step recovery doides and transistors.

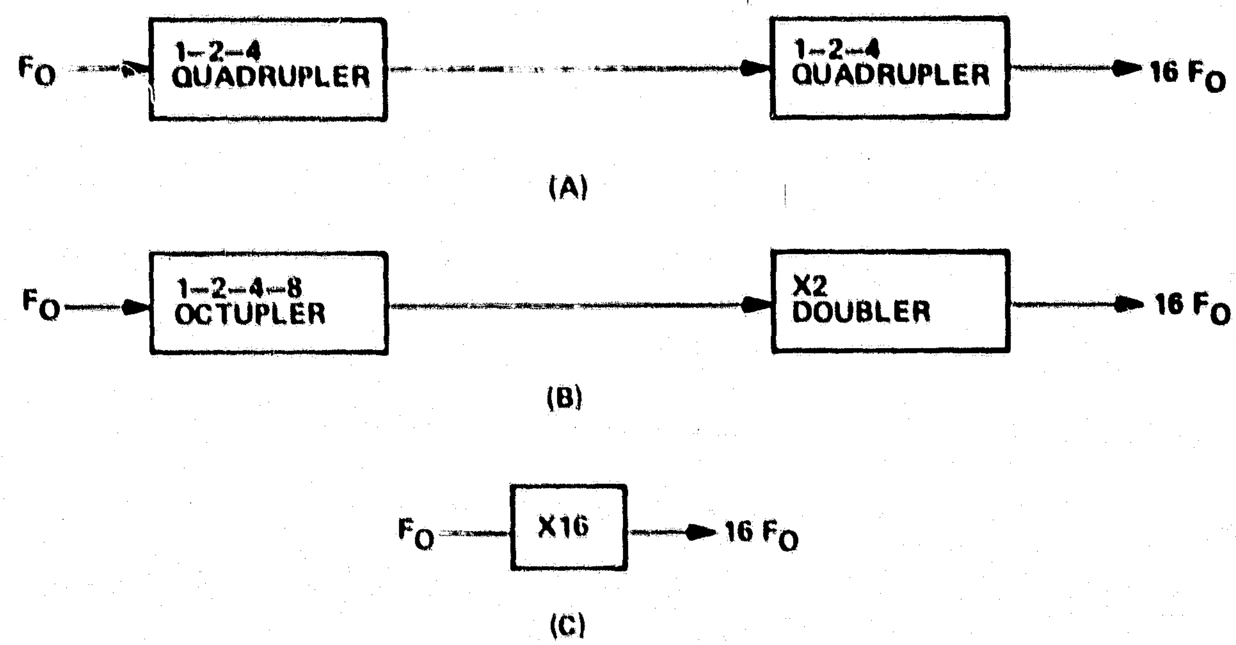

FIGURE 13. POSSIBLE X16 MULTIPLIER CONFIGURATIONS FOR MLS RECEIVER

VARACTOR MULTIPLIER

Frequency multiplication can be achieved by any device which has a non-linear component that causes the output voltage to be a non-linear function of the input voltage. A component commonly used for frequency multiplication is the varactor diode.

Figure 14 shows a model for the ideal PN junction varactor diode. Multiplication is possible because the depletion layer capacitance is a non-linear function of the applied voltage. The degree of non-linearity is determined by the fabrication technique. During device fabrication, the PN diode junction can be epitaxially grown or the impurities can be diffused into an appropriately doped substrate. Epitaxially grown junctions and constant source diffused junctions result in a junction region which has an abrupt change in the P to N type impurity region. Under these conditions the depletion layer capacitance is given by:

$$C_j = \frac{dQ}{dV} = \left[\frac{q\varepsilon N_a N_d}{2(N_a+N_d)}\right]^{1/2} V_T^{-1/2}$$

where: N_a/N_d = Acceptor/Donor Impurity Concentration
q = Electric Charge
ε = Permittivity

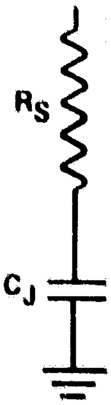

FIGURE 14. IDEAL VARACTOR DIODE MODEL

When the device is fabricated from a fixed impurity source an approximately linearly graded junction is obtained where the depletion layer capacitance is given by:

$$C_j = \frac{dQ}{dV} = \left(\frac{qaE^2}{12}\right)^{1/3} V^{-1/3}$$

where: q = Electric Charge
E = Permittivity
a = Impurity Gradient

Note that in both these cases the capacitance is a non-linear function of the voltage that appears across the depletion region. To maximize the conversion efficiency it is desirable that the exponent of V approaches 1/2. In actual devices fabricated by AEL using constant impurity concentration source diffusion techniques this exponent has exceeded 0.45.

The non-linearity of the junction capacitance is not the only term which must be considered in varactor multiplier design. The frequency and efficiency limiting component in the diode is the resistance in series with the junction capacitance. This resistance is primarily due to device geometry and material resistivity. Imprecise lead bonding and diode chip mounting will increase the value of this resistance.

When designing a multiplier using a varactor diode both the junction capacitance and series resistance must be taken into consideration. The multiplier efficiency becomes higher as the value of R_s decreases. To give an indication of the quality of a particular varactor diode, Penfield and Rafuse[1], have defined the cutoff frequency:

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[1] Penfield, P., and Rafuse, R.P. Varactor Applications, MIT Press, 1962.

$$f_{co} = \frac{S_{max} - S_{min}}{2\pi R_s} \qquad \text{usually } S_{max} >> S_{min} \text{ where } S_{max} = 1/C_{min} \qquad f_{co} = \frac{1}{2\pi R_s C_{min}}$$

The cutoff frequency gives an indication of the usable upper frequency limit of the varactor diode.

For higher order varactor multipliers and for greater multiplier efficiency, the varactor diode is often driven into the forward conduction region by the input voltage swing. The overdriven condition increases the overall non-linearity by introducing the effects of the PN junction diffusion capacitance. This effect is useful as long as the minority carrier lifetime is longer than the period that the diode is in the forward conduction region, and as long as the minority carriers are not driven so far into the region that they cannot be recovered. It should be noted that the diffusion capacitance is a very low Q capacitance effect. Under forward bias conditions, the depletion region width is minimum and the exposed epitaxial path through which the injected carriers travel is maximum; therefore, the instantaneous series resistance is significantly increased. Normally this increased series resistance effect is overshadowed by the circuit losses of the multiplier.

Varactor diode circuits comprise a majority of multiplier circuits designed today. Penfield and Rafuse[1] present an analysis which provides the designer with formulas that predict abrupt and linear graded junction multiplier performance. Burckhardt[2] did an analysis of varactors with arbitrary junction capacitance variation and drive level. The analysis should provide the designer with a technique to choose and characterize the best diode for the particular application, in addition to providing the foundation upon which the multiplier design is based.

Figure 13 showed three basic configurations considered for the MLS X16 multiplier. The basis for the multiplier design must be simplicity. This is absolutely essential in order to achieve a reliable, stable circuit at a reasonable cost. The circuit in Figure 13 is a single stage X16 multiplier which directly converts the input frequency to the desired 16th harmonic output frequency. This configuration is the most simple of the three choices, but is not really practical for a varactor diode because of the extremely high conversion loss.

The circuit in Figure 13b is more practical for varactor applications. The doubler circuit is relatively simple to build, and requires very little final tuning. Estimated

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[2] Burckhardt, C. B., "Analysis of Varactor Frequency Multipliers for Arbitrary Capacitance Variation and Drive Level," <u>Bell System Technical Journal</u>, Vol. XLIV, No. 4 (April 1965).

conversion loss for this circuit is approximately 2 dB. The disadvantage of Figure 13b circuit is that the 1-2-4-8 octupler has idler circuits at the second and fourth harmonics. In general, as the number of idlers of a multiplier is increased, the more efficient it becomes and the more complex and time consuming the tuning becomes. The complexity results because three parameters of the circuit must be tuned simultaneously; these are input match, output match and idler frequency. Since the diode impedance is (in general) dynamic, the tuning process is complicated by the fact that impedance levels change as a function of input and output power. During the tuning process it is of the utmost importance that the basic characteristic of the circuit being tuned is not destroyed. For example, the input matching circuit must prevent idler and output frequency currents from flowing in the input circuit. Should this characteristic be destroyed the output power and stability of the multiplier will become a function of the preceding driver stage's output impedance at the 2nd, 4th and 8th harmonic. Since the driver stage also has a dynamic output impedance, an almost impossible tuning situation occurs. Circuit designers faced with this type of problem often try to overcome it by using a circulator or pads between stages. This only makes the multiplier less efficient and more expensive.

To overcome some of the problems associated with the circuit in Figure 13b, the circuit in Figure 13a can be used. Here the 1-2-4-8 octupler is replaced by a 1-2-4 quadrupler. The circuit configuration eliminates the fourth harmonic idler, and thereby simplifies circuit tuning.

To conclude, a varactor diode multiplier in a configuration as shown in Figure 13a could be used in the MLS receiver. The predicted conversion loss for the two-stage circuit is 11 dB. The disadvantage of the circuit is that it uses two stages, the first of which would be at least partially lumped-element, increasing the assembly time. The fact that the circuit does consist of two individual stages will cause greater tuning time than a single stage circuit, and overall tuning will become more critical for stable operation.

STEP RECOVERY DIODE (SRD) MULTIPLIER

In a varactor multiplier, the depletion layer capacitance is the primary non-linear element that makes frequency multiplication possible. The diffusion capacitance is used to enhance multiplier operation. In the step recovery diode, the diffusion capacitance is the element which is used to achieve multiplication.

As previously stated, to use the diffusion capacitance effectively the minority carriers must not recombine when the diode is in the forward conduction region, and the minority carriers must be recoverable after the diode comes out of forward conduction. Step recovery diode fabrication is such that these conditions are optimally met. To prevent the minority carriers from diffusing out of reach, steep impurity profiles are doped into the SRD. These steep profiles generate fields which repel the minority carriers back toward the junction limiting penetration depth.

The usefulness of the SRD as a multiplier comes from the fact that the diode rapidly switches between 2 distinct impedance levels. Ideal circuit models of the SRD at these levels are shown in Figures 15a and 15b. Using the schematic diagram of an SRD multiplier in Figure 16 a qualitative discussion of the multiplier will be given. As shown in Figure 16, the multiplier is to be made up of three basic building blocks: The impulse generator, the input matching network, and the output resonator and band-pass filter.

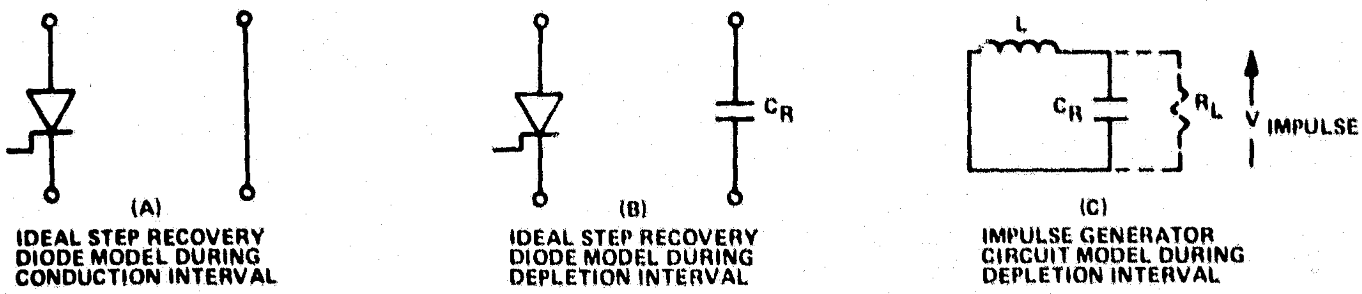


FIGURE 15. SCHEMATIC DIAGRAM OF SRD MULTIPLIER FIGURE

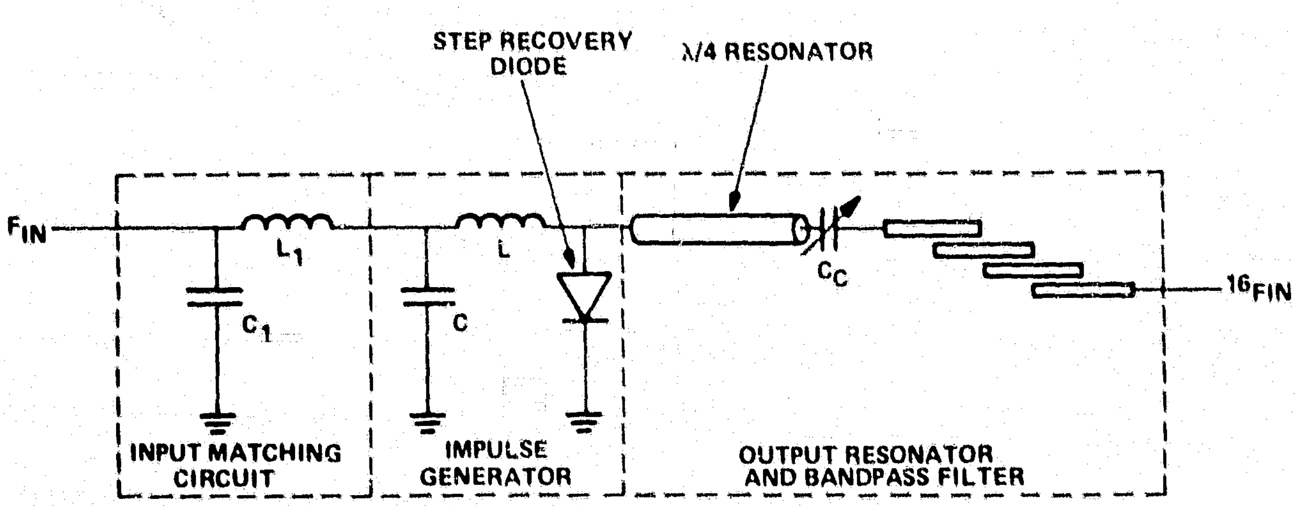


FIGURE 16. SCHEMATIC DIAGRAM OF X16 STEP RECOVERY DIODE MULTIPLIER

The heart of the multiplier is the impulse generator, which is made up of the SRD, L, and C. The impulse generator will generate a voltage pulse which is rich in harmonics once during each cycle of the input frequency. This voltage pulse is generated as follows. Because of the charge storage capabilities of the SRD, it is normally in the

conduction interval state shown in Figure 15a. This is a low impedance state during which the current in the impulse generator builds up a field around the charging inductor L. When all the current that has been stored by the SRD has been removed, the SRD will switch into the high impedance depletion interval model of Figure 15b. The bias on the SRD is adjusted so that the change in impedance level occurs when the current swing in the impulse generator is at its maximum negative point. The impulse generator circuit in the depletion interval is shown in Figure 15c. At the instant the SRD goes into the depletion state, the circuit current is going through a maximum negative point and the charge stored in L is maximum. The circuit will attempt to "ring" at a frequency determined by L and C_R with an initial voltage pulse across R_L equal to the reverse breakdown potential of the SRD. Only one half cycle of the ringing will appear across R_L because the SRD will again go into the conduction state when the voltage across it goes positive. The voltage pulse from the impulse generator is used to excite the resonator in the output resonator and bandpass filter section of the multiplier.

The output resonator and bandpass filter concentrate the energy of the voltage pulse generated by the impulse generator at the desired harmonic output frequency. The resonator is a one-quarter-wavelength shorted stub resonator which converts the voltage impulse into a damped harmonic that concentrates the energy at the desired output frequency. The resonator must be low-loss, so that all the available energy can be coupled to the output bandpass filter by the coupling capacitor C_c. Capacitor C_c is one of the adjustments that must be made to the multiplier. This coupling is critical to maximum power output, and is adjusted so that the resonator contains a damped harmonic which just dies out before the resonator is excited by the next impulse from the impulse generator.

The last circuit in the multiplier is the input matching circuit made up of L1 and C1. This circuit transforms the impedance of the impulse generator to the desired input impedance.

The SRD multiplier is the simplest multiplier for high order multiplication. The circuit has no adjustable idlers and has excellent frequency isolation between the output and input circuits. Only two adjustments are required. One, discussed above, is coupling capacitor, C_c, and the other is the diode bias level. The circuit is the most advantageous for ease of assembly and tuning. Its disadvantages are that the SRD costs slightly more than a varactor, and that special consideration must be given to diode mounting because of thermal dissipation.

The multiplier design that was used for the low cost MLS application is shown in Figure 16. At present, the step recovery diode is mounted in a glass package. This mounting introduces undesirable package parasitics and decreases multiplier efficiency, but greatly simplifies the multiplier assembly procedure and reduces the assembly cost. Using this technique necessitates the use of a two-stage amplifier driver, but the cost saving in the multiplier overshadows the cost of the additional amplifier.

TRANSISTOR MULTIPLIERS

Transistor frequency multipliers operate similarly to varactor multipliers. The basic difference is that the transistor multiplier actually provides gain, thus combining the standard two-stage power amplifier/multiplier configuration.

The basic transistor multiplier circuit provides multiplication through the use of the non-linear collector to base junction capacitance. The efficiency is a function of the cutoff frequency of this varactor which is given by:

$$f_{co} = \frac{1}{2\, C_{min} R_{EQ}}, \text{ where}$$

R_{EQ} = mainly due to series collector resistance and base spreading resistance

C_{min} = minimum value of collector base junction capacitance

This type of multiplier is excellent for use in low frequency (less than 1 GHz) low order multipliers because it eliminates the need for a two-stage amplifier/multiplier combination. The transistor multiplier's main disadvantage is stability problems, which occur because the non-linear multiplying element is imbedded in the fundamental frequency gain device and is subject to the undesirable parasitic elements of that device. Because the non-linear device is imbedded, it becomes more difficult to control the undesirable parasitic currents directly at the device terminals. Several types of stability problems are associated with this type of multiplier; these include low frequency instability, high frequency instability, and parametric instability.

Low frequency instability is a common problem with amplifiers in general. It is caused by the transistor's gain increasing as a function of decreasing frequency. Any low frequency resonant loop in the amplifier can cause oscillations. The problem is normally overcome by providing low Q DC return paths and careful power supply decoupling.

High frequency instability is a greater problem. Higher order multipliers, for maximum efficiency, require several idler circuits in the collector circuit to encourage the flow of idler currents. Because the emitter base matching circuit is a reactive load to the transistor at the idler frequencies, feedback from the output through the collector emitter junction capacitance at high frequencies can cause undesirable high frequency oscillations. This effect can be difficult to overcome, but can be eliminated by minimizing the collector emitter junction capacitance and changing the reactive loading on the transistor at the frequency at which it wants to resonate.

Parametric instabilities are another form of high frequency instability. The collector base junction capacitance can appear as an effective negative resistance by the pump action of the high frequency output signal. Should any low frequency instabilities

lie in the region of this negative resistance they will be amplified causing a regenerative feedback effect. If the magnitude of the negative resistance generated by the junction capacitance is larger than the magnitude of the positive resistance, the device will become potentially unstable, oscillating with changing bias level or load changes. Parametric effects are difficult to overcome, especially for high frequency multipliers where the Q of the junction capacitance is fairly high.

From the previous discussion it can be seen that the transistor multiplier is the most unstable multiplier of the various types considered, especially when operating under high order, high frequency conditions.

Cost/performance trade-offs. - The previous paragraphs discussed three types of multipliers in detail. Figure 17 shows, in outline form, the advantages and disadvantages of each type. Based on these facts, the SRD multiplier was chosen as the most cost-effective approach.

Cost is one of the primary considerations in choosing the multiplier type. The total multiplier cost includes parts, assembly, and tuning cost. The SRD parts cost slightly more than that of the transistor and varactor multiplier because the diode cost is more than that of transistor or varactor diodes. The additional parts cost of the SRD is greatly offset by the low assembly and tuning costs.

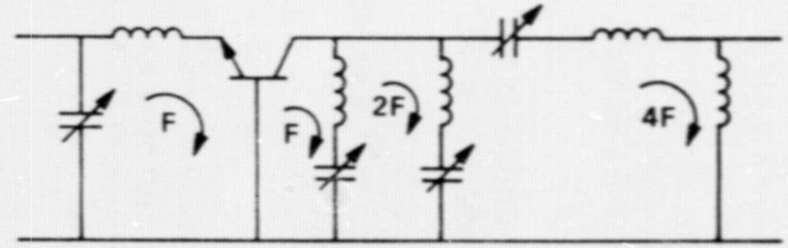
Circuit performance also favors the SRD as the multiplier choice. The SRD is much more stable than the transistor multiplier, and its stability is not as dependent on circuit tuning as it is with the varactor and transistor multipliers.

The SRD multiplier is easier to implement than the transistor and varactor multiplier. For maximum efficiency in high order transistor and varactor multipliers, several idler circuits must be added. Idler circuits increase circuit complexity and greatly increase tuning time. At most, the SRD multiplier can be considered to have one broadband idler which requires absolutely no tuning.

The simple SRD multiplier circuit makes it more reliable than the transistor or varactor multiplier. Since it has no tuned idlers, it is less susceptible to environmental drift. Its reliability is far greater than the transistor multiplier, because it has lower junction dissipation. Its dissipation is lower because it is a more efficient multiplier and because there is no additional DC junction dissipation as there is in the transistor multiplier.

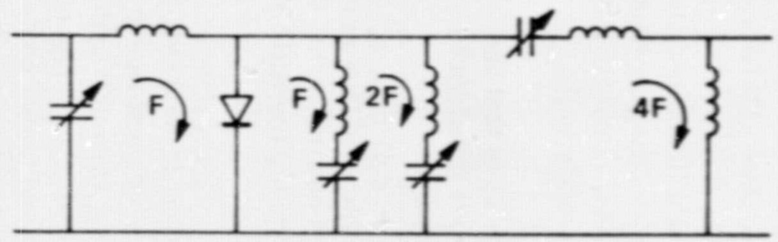
The SRD multiplier is the most cost effective type of multiplier to use for the MLS receiver. Optimum performance is achieved when the diode is used in chip form to minimize undesirable package parasitics. The diode in chip form greatly increases assembly complexity and significantly increases multiplier costs. To simplify the assembly procedure, the diode is used in a glass package. This package degrades multiplier performance by decreasing the conversion efficiency. Since the biased mixer

A.) TRANSISTOR MULTIPLIERS
ADVANTAGES
1.) MULTIPLICATION IN AN AMPLIFIER CHAIN
DISADVANTAGES
1.) LIMITED ORDER OF MULTIPLICATION
2.) COMPLEX CIRCUIT DESIGN AND TUNING
3.) LOW AND HIGH FREQUENCY STABILITY PROBLEMS
4.) HIGH THERMAL DISSIPATION IN HIGH ORDER MULTIPLIERS
5.) PROBABLE HIGH COST IN THIS FREQUENCY RANGE



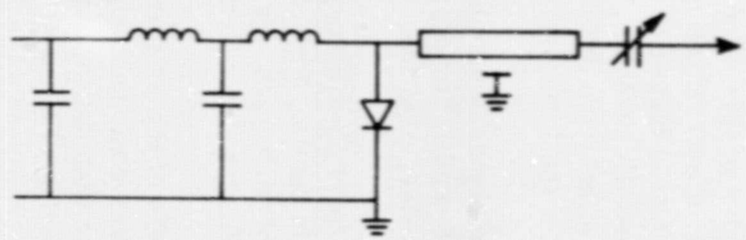
TRANSISTOR QUADRUPLER (1, 2, 4 CONFIGURATION)

B.) VARACTOR DIODE MULTIPLIERS
ADVANTAGES OVER TRANSISTOR MULTIPLIERS
1.) MORE EFFICIENT
2.) MORE STABLE
3.) LESS THERMAL DISSIPATION
4.) SLIGHTLY LOWER COST
DISADVANTAGES
1.) COMPLEX CIRCUIT DESIGN AND TUNING
2.) STABILITY A FUNCTION OF TUNING



VARACTOR QUADRUPLER (1, 2, 4 CONFIGURATION)

C.) STEP RECOVERY DIODE MULTIPLIERS
ADVANTAGES
1.) SIMPLE CIRCUIT
2.) VERY LITTLE TUNING
3.) STABLE
DISADVANTAGES
1.) DIODE COSTS SLIGHTLY HIGHER THAN VARACTOR



HIGH ORDER SRD MULTIPLIER

FIGURE 17. MULTIPLIER TRADE-OFFS

requires a power level of as low as -7 dBm, the decreased conversion efficiency can be overcome by increasing the multiplier RF drive level.

Filter requirements and purpose. - Two bandpass filters are required in the RF head as shown in Figure 18. One filter is required for LO filtering and the other for RF filtering. The LO filter is needed to pass the X16 multiplier product and yet reject the X15 and X17 products. The RF filter is needed to pass the RF signal band and reject any radiated LO signal. The filter will also reject the image frequency band; i.e., the image band consists of LO-IF product, whereas, the RF band consists of LO + IF product.

FILTER SPECIFICATIONS

LO Filter - (See also filter mask in Figure 22)

PASSBAND: 4.8702 to 4.9299 GHz (X16 Product)

REJECT BAND: 4.5658 to 4.6218 GHz (X15 Product) and below
5.1746 to 5.2380 GHz (X17 Product) and above

REJECTION: 38 dB Minimum

VSWR (IN PASSBAND): 1.5:1 Maximum

INSERTION LOSS: 2.5 dB

RF FILTER - (See also filter mask in Figure 22)

PASSBAND: 5.031 to 5.0907 GHz

REJECT BAND: 4.8702 to 4.9299 GHz (LO)
4.7094 to 4.770 GHz (Image)

REJECTION: 40 dB Minimum at LO
62 dB Minimum at Image

VSWR (IN PASSBAND): 1.5:1 Maximum

INSERTION LOSS: 3.0 dB

The physical size of the filters must necessarily be small, since both must fit into a space on the order of 6 inches by 3 inches by 2 inches along with other circuitry. They must be lightweight and inexpensive to manufacture. Each filter should be rectangular in shape, relatively thin and consume little area on the circuit board. A typical size guideline is 2.5 inches by 0.5 inch by 0.2 inch.

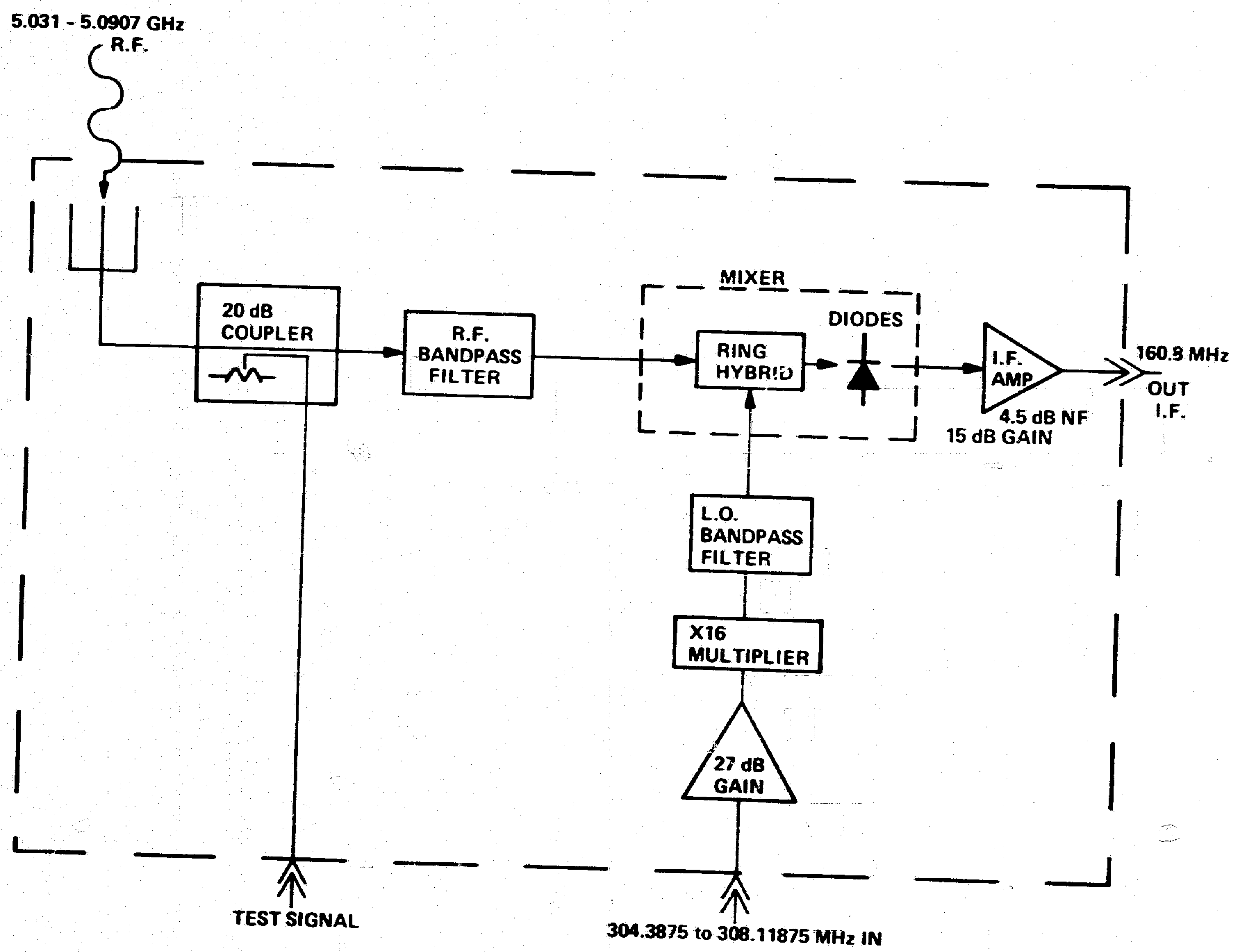


Figure 18. MLS REMOTE RF HEAD BLOCK DIAGRAM

Both filters interface with the down converting mixer. In addition, the RF filter must interface with a test signal coupler and the LO filter interfaces with the X16 multiplier.

Types of filters considered. - Coaxial filters can be built sturdily and with relatively low insertion loss. Dielectric supports are required which adversely affect the Q as compared to a filter surrounded by air only. Also, coaxial filters require precision parts; therefore, machining and assembly become prohibitively expensive. A coaxial filter is bulky, has a poor form factor and more than doubles the proposed size.

A waveguide filter would have the lowest insertion loss and the highest unloaded Q of all the types considered. It can be built quite sturdily; however, it is extremely bulky and expensive to manufacture.

Microstrip represents an attractive solution, since it yields the smallest physical size of those types considered. Its size is approximately one-half of the proposed stripline design. However, alumina is a relatively expensive material and it is quite brittle. It may be subject to fracture under severe vibration.

A filter made in air line represents a lightweight construction. The space required for this type of filter is about twice that of the stripline filter proposed. The circuit is photoetched on Kapton and suspended between two channelized ground planes. The channel is hydraulically stamped in the ground plane metal and the plates riveted together. Tooling costs for this approach are high, but the approach may yield the least expensive manufacturing costs of any considered. Stripline was selected over this approach because of its size. Also, because the substrate is suspended in air, it may be quite sensitive to vibration, causing filter mistuning or possible fracture.

Stripline affords a workable compromise in characteristics for fabrication of the filter. The material selected is teflon-glass, 3M type K-6098 GT, with a thickness of 0.031 inch. It is flexible and easily cut to size; although its flexibility causes the filter to be subject to mistuning, the proposed construction will support the material so that this problem will not be of concern. Assembly is accomplished with ease and material costs are moderate.

Selection of filter type. - Considering the factors outlined in the previous discussion, it was determined that the stripline filter offered the best compromise in overall characteristics; therefore, the stripline filter was selected.

Each filter consumes an area of about 2.34 inches by 0.19 inch on the stripline surface. The materials cost for the space required for each filter is about 15 cents. Construction of each filter involves a photolithographic process followed by a bonding of the two halves together under heat and pressure. In quantity, the operation can be done quite inexpensively.

The proposed design is an edge-coupled resonator configuration. The resonator Q's of this scope are less than those obtained with coaxial technique or perhaps less than the gap-coupled resonator design. The reasons for the choice over the coaxial design has already been discussed; however, the gap-coupled design was rejected due to size constraints. The gap-coupled design is approximately twice as long as the edge-coupled design. The edge-coupled resonator filter will meet or exceed the specifications set forth previously.

The filters will interface directly with the other components in the circuitry, since all components will be included on the same photographic mask.

Nothing short of fracture of the entire stripline package will cause either filter to fail, provided that proper care is taken in assembly to ensure that no foreign particles are introduced between the resonator gaps.

The reject band attenuation possible in either coaxial or waveguide filters is not possible in stripline. Stripline will also tend to be more lossy in the passband. Therefore, with lower cost stripline, we produce a smaller package with somewhat less than optimum RF performance.

Mixer Requirements (see figure 22)

The mixer will have a maximum of 8 dB conversion loss.

The 2 x 2 mixer spurious response will be 87 dB below the IF output signal at an RF input level of -30 dBm.

The mixer will provide 12 dB of LO rejection at the RF port entering it.

The mixer will require no more than +7 dBm of LO drive to obtain the specified 8 dB conversion loss in an unbiased condition. Biased, the mixer will be capable of operating with -7.0 dBm LO input with 8 dB conversion loss.

The mixer is to operate with an input frequency range of 5.031 to 5.0907 GHz and a local oscillator frequency range of 4.8702 to 4.9299 GHz. The output mixer product is to be 160.8 MHz, which is the intermediate frequency.

The physical size of the mixer must be small in order to fit reasonably well within the other circuitry in the RF head. It must be lightweight for aircraft applications, and

be inexpensive to manufacture. A stripline-type mixer is required in order to facilitate adaptation to the other stripline circuitry. A typical size guideline is 1 inch by 1 inch by 0.2 inch.

Mixer types considered. - Several mixer configurations are available. A short summary of the characteristics of some of the main types are listed below.

A single ended mixer is constructed using only one diode. It has the lowest LO drive requirement of all the mixers considered here, and its conversion loss is approximately 5 to 7 dB. The LO to RF isolation is very much dependent upon the external frequency selection elements; therefore, in general, the isolation is quite poor.

A single balanced mixer uses two diodes and a 3 dB hybrid power splitter. This type of mixer requires twice the LO drive power as compared to the single ended variety, and its conversion loss is about the same; i.e., 5 to 7 dB. The LO to RF isolation is fair (approximately 10 to 15 dB), dependent upon whether a 90-degree hybrid or a 180-degree hybrid is used. A 180-degree hybrid will yield the higher isolation.

A double balanced mixer requires four diodes, and the RF and LO input is via transformers. As compared to a single ended mixer, a double balanced mixer requires four times the LO drive power. Its conversion loss is fair (approximately 7 to 9 dB), and its LO to RF isolation is approximately 30 dB, which is very good.

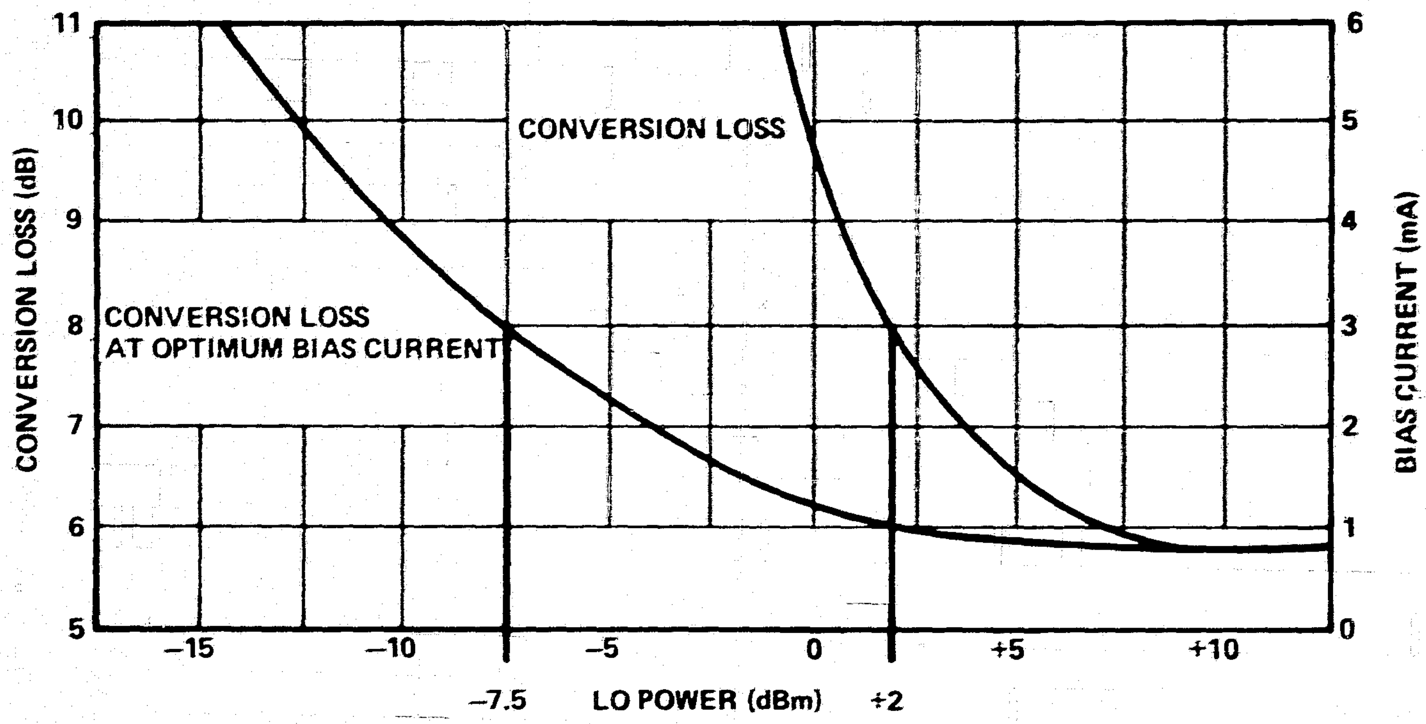
For all of the mixers named above, the LO drive requirement may be reduced by DC-biasing the diodes. Typically, the LO drive power may be reduced 9.5 dB and still maintain the same conversion loss if the diodes are biased (see Figure 19). Biasing will also reduce the conversion loss if the drive power is not reduced and, consequently, result in a reduction in the mixer noise figure. Coils must be attached to the RF lines in the mixer to supply the bias currents, thereby increasing the mixer cost slightly.

Selection of mixer type (see figure 30). - The single ended mixer was rejected due to its poor isolation. The double balanced mixer was rejected because of its complexity in construction and the added expense of additional diodes. Also, the double balanced mixer requires excessive LO drive and has relatively high conversion loss. Therefore, the single balanced mixer was selected for this application.

The 90-degree hybrid version of the single balanced mixer was chosen of the two types available. In comparison, the 90-degree version has the lower conversion loss and better VSWR, although it has the poorer LO to RF isolation. Also, a 180-degree hybrid is somewhat larger, and its form factor is not as symmetric as the 90-degree hybrid.

The single balanced mixer is inexpensive, with the cost primarily being that of the diodes. Its cost is roughly twice that of the single ended mixer, but less than half of the cost of the double balanced mixer.

TYPICAL CONVERSION LOSS AND BIAS CURRENT VERSUS LO POWER FOR 90° HYBRID BIASED MIXER.



BY THE GRAPH ABOVE, FOR 8 dB CONVERSION LOSS:

1) BIASED. USING –7.5 dBm L.O. DRIVE AND 3 mA OF BIAS CURRENT THIS IMPLIES A) SUPPLYING A VOLTAGE INTO THE STRIPLINE PACKAGE THROUGH A FEED THROUGH B) CHOOSING AN RF CHOKE TO ATTACH THE STRIPLINE.

2) UNBIASED. USING +2 dBm L.O. DRIVE. THIS IMPLIES GROUNDING THE DIODES TO D.C. THIS MEANS CONNECTING THE STRIPLINE TO GROUND THROUGH AN RF CHOKE.

FIGURE 19. BIASED VERSUS UNBIASED MIXER TRADE-OFFS

MIXER TYPE	NO OF DIODES (1)	VSWR (2)	CONVERSION LOSS (3)	LO/RF ISOLATION (4)	BIAS	SPURIOUS REJECTION (5) $\|m-n\| = 1$	HARMONIC SUPPRESSION (6)	INTERCEPT POINT (7) dBm	DYNAMIC RANGE	IF BANDWIDTH	IMAGE FOCUSING PORT (9)
90° HYBRID	2	GOOD	LOWEST	POOR	NO	POOR	POOR	-15	HIGH	WIDE	LO
	2	GOOD	LOWEST	POOR	YES	FAIR	FAIR	-30(8)	HIGHEST	WIDE	LO
180° HYBRID	2	POOR	LOW	GOOD	NO	POOR	GOOD	-15	HIGH	WIDE	RF
	2	POOR	LOW	GOOD	YES	FAIR	GOOD	-15	HIGH	WIDE	RF
	2	POOR	LOW	GOOD	YES	FAIR	GOOD	-30(8)	HIGHEST	WIDE	RF
QUAD. FED	4	GOOD	LOW	VERY GOOD	NO	GOOD	FAIR	-18	HIGH	WIDE	INTERNAL LOAD
DUAL DOUBLE BALANCED	4	POOR	LOW	VERY GOOD	NO	GOOD	VERY GOOD	-18	HIGH	WIDE	RF
	4	POOR	LOW	BEST	NO	GOOD	VERY GOOD	-18	HIGH	EXTREMELY WIDE	RF

NOTES:

(1) 2-DIODE TYPES REQUIRE +7 dBm LO POWER FOR BEST PERFORMANCE. 4-DIODE TYPES REQUIRE +10 dBm LO POWER

(2) VSWR: POOR: 2.5:1 typ
GOOD: 1.3:1 typ

(3) CONVERSION LOSS: LOWEST: 5–7 dB typ
LOW 7–9 dB typ

(4) LO/RF ISOLATION: POOR: 10 dB typ
GOOD: 20 dB typ
VERY GOOD: 25-30 dB typ
BEST: 35-40 dB typ

(5) mxn SPURIOUS REJECTION: WHERE $|m-n| = 1$; i.e., 1X2, 2X1, 2X3, 3X2, ETC.
POOR: PARTIAL REJECTION OF MOST $|m-n| = 1$ SPURS
FAIR: PARTIAL REJECTION OF MOST $|m-n| = 1$ SPURS (BIAS ADJUST WILL SUPPRESS SOME SPURS EVEN FURTHER)
GOOD: POTENTIALLY REJECTS ALL $|m-n| = 1$ SPURS

(6) HARMONIC SUPPRESSION: POOR PARTIAL REJECTION OF LO/RF EVEN HARMONICS
FAIR: PARTIAL REJECTION OF LO/RF EVEN HARMONICS (BIAS ADJUST WILL SUPPRESS SOME HARMONICS EVEN FURTHER.)
GOOD: CAN REJECT ALL LO EVEN HARMONICS.
VERY GOOD: CAN REJECT ALL LO AND RF EVEN HARMONICS

(7) INTERCEPT POINT: TYPICAL THIRD ORDER INTERCEPT POINT IS 6 TO 9 dB ABOVE THE LO POWER.

(8) THIS INTERCEPT POINT CAN ONLY BE ACHIEVED BY USING THE OPTIMUM LOAD LINE BIASING TECHNIQUE AND INCREASING THE LO POWER TO APPROXIMATELY +23 dBm.

(9) IMAGE FOCUSING: DEFINES WHERE IMAGE SIGNAL ENERGY IS FOCUSED, LO PORT, RF PORT, OR TO INTERNAL TERMINATION. (WHERE THIS IMAGE SIGNAL IS FOCUSED CAN AFFECT MIXER PERFORMANCE IN PHASE AND AMPLITUDE TRACKING SYSTEMS.

FIGURE 20. PERFORMANCE COMPARISON OF FOUR BASIC MIXER TYPES

MIXER TYPE	NO OF DIODES (1)	VSWR (2)	CONVERSION LOSS (3)	LO RF ISOLATION (4)	BIAS	SPURIOUS REJECTION (5) $\lvert m-n \rvert = 1$	HARMONIC SUPPRESSION (6)	INTERCEPT POINT (7) dBm	DYNAMIC RANGE	IF BANDWIDTH	IMAGE FOCUSING PORT (9)
90° HYBRID	2	GOOD	LOWEST	POOR	NO	POOR	POOR	-15	HIGH	WIDE	LO
	2	GOOD	LOWEST	POOR	YES	FAIR	FAIR	-30 (8)	HIGHEST	WIDE	LO
180° HYBRID	2	POOR	LOW	GOOD	NO	POOR	GOOD	-15	HIGH	WIDE	RF
	2	POOR	LOW	GOOD	YES	FAIR	GOOD	-15	HIGH	WIDE	RF
	2	POOR	LOW	GOOD	YES	FAIR	GOOD	-30 (8)	HIGHEST	WIDE	RF
QUAD FED	4	GOOD	LOW	VERY GOOD	NO	GOOD	FAIR	-12	HIGH	WIDE	INTERNAL LOAD
DUAL DOUBLE-BALANCED	4	POOR	LOW	VERY GOOD	NO	GOOD	VERY GOOD	-18	HIGH	WIDE	RF
	4	POOR	LOW	BEST	NO	GOOD	VERY GOOD	-12	HIGH	EXTREMELY WIDE	RF

NOTES

(1) 2-DIODE TYPES REQUIRE +7 dBm LO POWER FOR BEST PERFORMANCE.
4-DIODE TYPES REQUIRE +10 dBm LO POWER

(2) VSWR: POOR: 2.5:1 typ
GOOD: 1.3:1 typ

(3) CONVERSION LOSS: LOWEST: 5–7 dB typ
LOW 7–9 dB typ

(4) LO RF ISOLATION: POOR: 10 dB typ
GOOD: 20 dB typ
VERY GOOD: 25-30 dB typ
BEST: 35-40 dB typ

(5) $m \times n$ SPURIOUS REJECTION: WHERE $\lvert m-n \rvert = 1$, i.e., 1X2, 2X1, 2X3, 3X2, ETC
POOR: PARTIAL REJECTION OF MOST $\lvert m-n \rvert = 1$ SPURS
FAIR: PARTIAL REJECTION OF MOST $\lvert m-n \rvert = 1$ SPURS (BIAS ADJUST WILL SUPPRESS SOME SPURS EVEN FURTHER)
GOOD: POTENTIALLY REJECTS ALL $\lvert m-n \rvert = 1$ SPURS

(6) HARMONIC SUPPRESSION: POOR PARTIAL REJECTION OF LO/RF EVEN HARMONICS
FAIR: PARTIAL REJECTION OF LO/RF EVEN HARMONICS (BIAS ADJUST WILL SUPPRESS SOME HARMONICS EVEN FURTHER.)
GOOD: CAN REJECT ALL LO EVEN HARMONICS.
VERY GOOD: CAN REJECT ALL LO AND RF EVEN HARMONICS.

(7) INTERCEPT POINT: TYPICAL THIRD ORDER INTERCEPT POINT IS 6 TO 9 dB ABOVE THE LO POWER.

(8) THIS INTERCEPT POINT CAN ONLY BE ACHIEVED BY USING THE OPTIMUM LOAD LINE BIASING TECHNIQUE AND INCREASING THE LO POWER TO APPROXIMATELY +23 dBm

(9) IMAGE FOCUSING. DEFINES WHERE IMAGE SIGNAL ENERGY IS FOCUSED, LO PORT, RF PORT, OR TO INTERNAL TERMINATION. (WHERE THIS IMAGE SIGNAL IS FOCUSED CAN AFFECT MIXER PERFORMANCE IN PHASE AND AMPLITUDE TRACKING SYSTEMS.

FIGURE 20. PERFORMANCE COMPARISON OF FOUR BASIC MIXER TYPES

The mixer is constructed in the stripline package integrated with a test coupler and the filters. The diodes are then soldered in place on the mixer. The hybrid will interface directly with the two filters feeding the required signals to the mixer. Diode attachment is accomplished through a hole in one side of the stripline package after the package has been bonded. The hole is then filled in after the part has been attached.

Purchased in a quantity of 4000 pieces, Schottky barrier diodes cost approximately $1.50 each. A single balanced mixer has 10 dB LO to RF isolation inherent in the construction. In order to obtain the required isolation in a single ended mixer, more elaborate frequency selection networks are required.

It is possible to bias this mixer, which would involve the slight added expense of insertion of the bias. This expense is traded for lowered LO drive resulting in lowering the cost of the local oscillator, which is quite significant at 5 GHz, due to the drive requirement being as low as -7.0 dBm.

Microwave Packaging Trade-Offs

Two packaging approaches were considered. The one that was discarded has the RF head separate from the antenna and mounted inside the aircraft in close proximity to the antenna. This design required the installation of two separate packages, plus the antenna in the aircraft and cabling between them. The added loss of the cabling was undesirable. Due to the degradation of performance, the added cost for two installations, and the added cost to the manufacturer and distributors of inventorying two separate units, this approach was deemed unadvisable.

Integration of the antenna with the RF head appears to be the best method of construction for optimization of performance, minimum manufacturing costs and ease of installation.

The integrated configuration shown in Figure 21 in exploded art form has been chosen as the best solution to the problems of performance, manufacturing, and field installation.

The RF head/antenna integrated assembly is composed of an RF subassembly, a bottom enclosure, and a radome. The RF subassembly consists of a stripline assembly with an integral antenna, an amplifier and X2 multiplier on a printed wiring board and an x8 step recovery diode multiplier.

The bottom enclosure contains the connectors to cable the RF head to other units of the system. The radome is a plastic molding that houses all of the components and provides means to attach the RF head to an aircraft. Figure 22 shows the basic concept of the RF head.

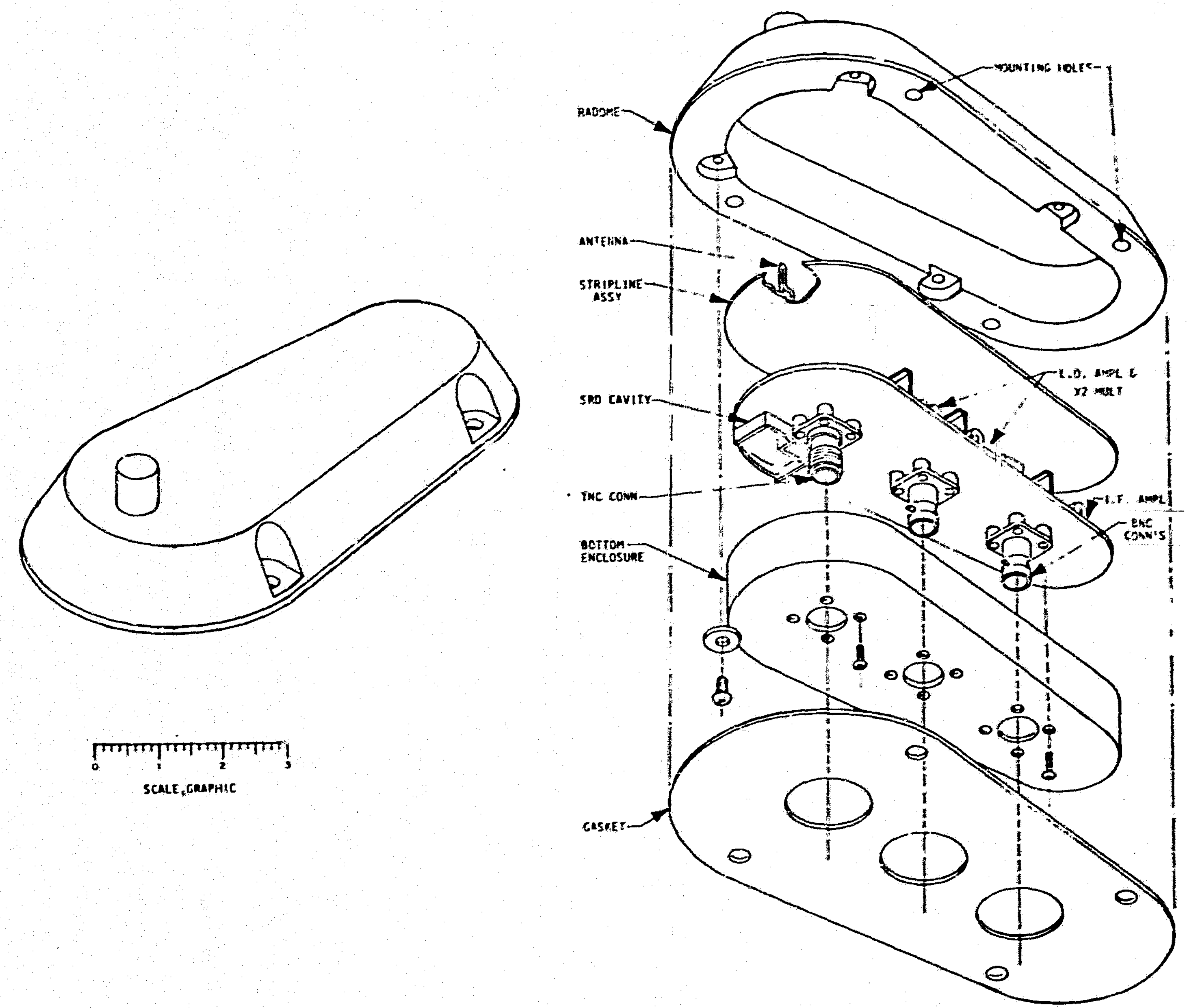


FIGURE 21. DETAILED BREAKAWAY DRAWING OF RF HEAD FIGURE

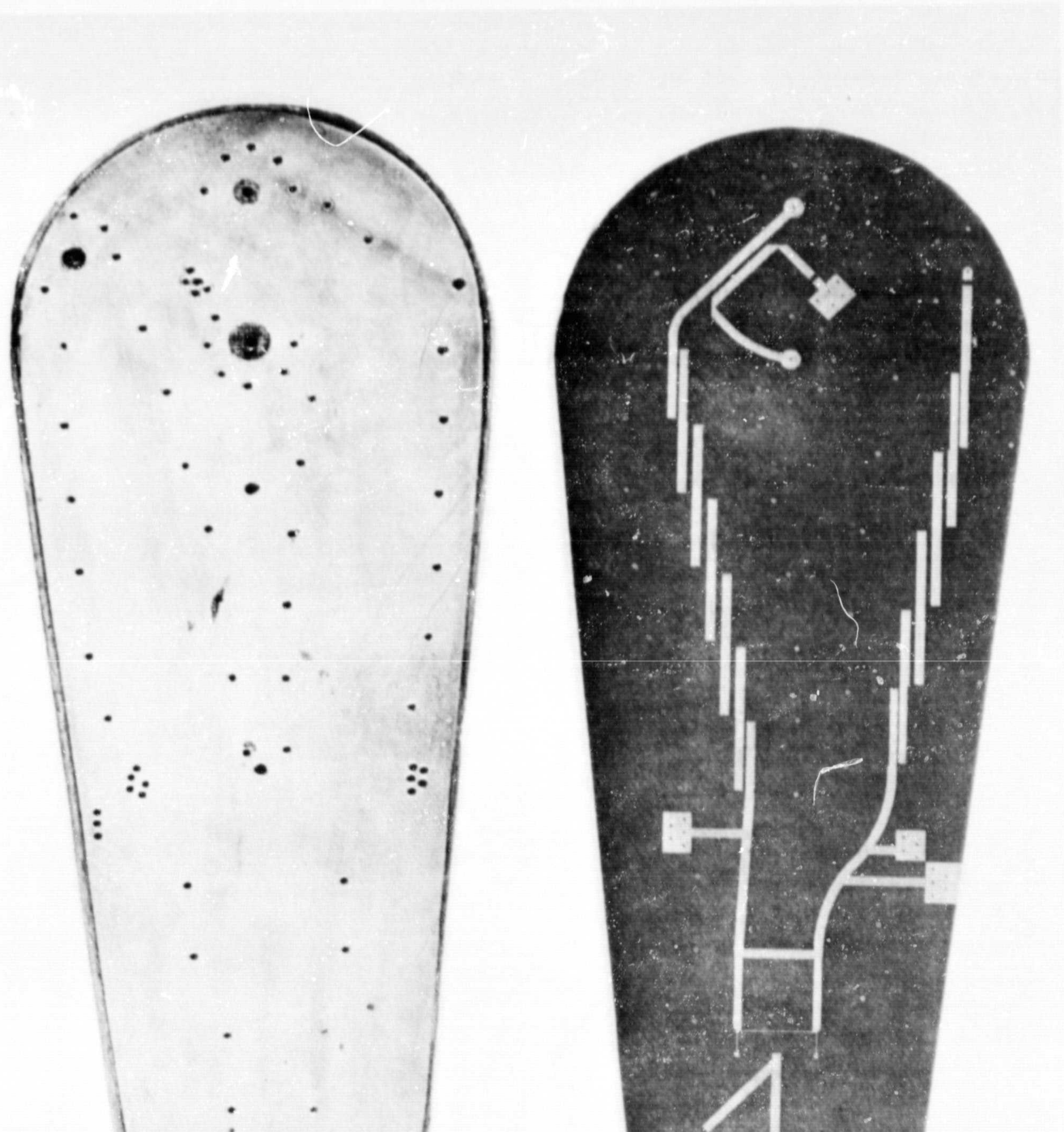


FIGURE 22. MICROWAVE STRIPLINE SUBASSEMBLY

Stripline assembly. - After consideration of various materials for the stripline assembly, 3M products K-6098 Teflon-Glass cloth laminate was initially chosen as the best compromise between material costs and electrical performance. To construct the package, two modes of assembly were analyzed. The first method (Method 1) consists of two copper-clad dielectric boards between two aluminum pressure plates. The sandwich is assembled with rivets or eyelets that are located so that they provide mode suppression and electrical paths, as required, as well as mechanical fastening.

A second method (Method 2) of manufacturing the stripline that eliminates the need for the pressure plates and mechanical fasteners is accomplished by bonding the two dielectric boards together with a bonding film compatible with the dielectric material. After bonding, mode suppression and electrical paths are provided by plating copper through holes in the dielectric boards. The copper plating also covers the edges of the dielectric boards, thus sealing the assembly.

After researching the problem it was determined that Method 2 was not only slightly less expensive to manufacture, but also would provide a package which would provide highly consistent electrical performance from assembly to assembly in a production run, thus reducing rework costs, scrap costs, and testing time, as well as providing high reliability. In addition, Method 1 would require sealing for humidity and (possibly) RF shielding, thereby adding to its cost; Method 2, by means of its construction, would already have these benefits built in.

The stripline package also provides the basic ground plane for the antenna. There exists the possibility of a resonant cavity being formed in the space between the stripline assembly and the connector mounting plate that would be detrimental to optimum performance of the system. This space must, therefore, be shielded. The shielding will be provided by flanging the connector mounting plate up to the stripline assembly thus completing the ground plane of the antenna.

Printed wiring assembly. - The LO and IF amplifiers are of printed wiring construction on a common substrate. There are no stringent electrical requirements imposed on the selection of the substrate material; therefore, the material selection is based upon environmental consideration, processing limitations, and cost.

There are many printed wiring substrate materials from which to choose. These range from the simple inexpensive paper-base phenolics through the exotic fiberglass polyimides, teflon, and silicones. The least expensive paper phenolics are usually hygroscopic and lack good bond strength. The properties of the exotic materials are not required for this application. Therefore, the chosen substrate material is one that provides the bond strength, temperature resistance, and non-absorbency required for use in the uncontrolled environment of the external surface of an aircraft. It also lends itself to manufacturing ease and is relatively inexpensive in production quantity.

Some of the paper and cloth base phenolic and melomine resin material were evaluated along with the epoxy fiberglass materials. Although some of the better

grade paper phenolics were found to be suitable for this application, further investigation disclosed that there is very little difference in cost between these materials and the higher quality glass epoxy represented by Nema Grade G-10.

Most PC manufacturers are very well versed in the processing of G-10, which is universally available. G-10 was chosen because it is the most cost-effective of the materials investigated. The bottom enclosure is a drawn aluminum can that forms an enclosure for the RF subassembly, provides a skirt for the antenna ground plane and supports the three RF interface connectors.

Integrated assembly. - The LO and IF amplifiers are constructed on a printed wiring (PW) board using conventional PC manufacturing techniques and materials. The PW Board is attached to the bottom side of the stripline assembly with swaged standoffs.

Several final assembly methods have been explored. One method uses bosses molded into the plastic housing passing through the stripline assembly and PW Board to the connector mounting plate to accept self tapping screws. The disadvantages of this method are (a) the difficulty of molding bosses without dimpling of the outer surface, (b) the controls required on assembly lines to ensure that the screws are properly installed, and (c) the possibility of untrained personnel removing the hardware and radome and possibly damaging the RF head.

Another method requires tabs on the connector plate can for screws penetrating into the side walls of the housing. This method eliminates the disadvantages of (a) but does not alleviate the problems of (b) and (c). It also has some disadvantages of its own; e.g., the tabs form openings in the skirt which may affect its shielding integrity and make sealing of the unit more difficult.

After consultation with several plastic molding manufacturers, it has been determined that the dimpling problem noted above can readily be overcome by extending the trailing edge of the fin that houses the antenna. Therefore, an assembly technique that makes use of the bosses in the radome but eliminates the need for separate pieces of hardware has been decided upon. The bosses will have a shoulder to position enclosure and have an extrusion protruding through the enclosure which is spin welded to make a tight, strong assembly.

Environmental considerations. - The entire microwave package, when mounted on the aircraft, will be sealed by the elastomeric gasket against the external environment so that the components will be protected from weather. The materials selected will be able to operate satisfactorily in temperatures from approximately -55 to +71 degrees Centrigrade under all humidity conditions. The package must withstand constant exposure to sunlight without deterioration and be rugged enough physically to withstand handling during maintenance and cleaning operations on the aircraft.

Throughout the design and construction of this assembly, components and material were individually chosen to withstand the environmental rigors to which the RF head is

subjected. Components such as transistors, capacitors, and resistors, when installed and conformal-coated, will withstand a humid environment. The stripline assembly, by the nature of its construction, is a sealed unit and is able to withstand humidity, temperature, etc., experienced in its end use.

The selection of materials, components, processes and manufacturing techniques employed in the design of the RF head were chosen to enable it to meet the environmental performance of DO 160.

Interface with antenna. - The antenna will be physically mounted to its ground plane and be an integral part of the stripline package. The antenna, of course, will stand above the ground plane. The dielectric material must enclose the antenna portion of the package to provide physical protection without interfering with its operation.

Aircraft interface mechanical considerations. - The prime mechanical interface consideration concerning the selection of the installation position on the aircraft is to select a surface as near to flat as possible in a section on the aircraft which is easily accessible from the inside to simplify making the necessary cable connections. By picking a flat surface, the basic mounting flange shape can be adapted to various aircraft with a simple elastomeric gasket/adapter. The only modification to the aircraft skin will be the drilling of mounting holes for the doubler plate and three circular holes to provide clearance for the connectors.

To install the AEL designed RF head into the aircraft, three holes are required to allow the connectors to pass through the skin. Four mounting holes are required to fasten the RF head to the aircraft structure. A resilient gasket will be provided with the RF head to weather-seal the openings. The gasket will also enable the RF head to conform to slightly curved surfaces. Four #8 screws are required for mounting.

The RF head utilizes a molded radome/housing which completely encloses the microwave package and antenna, and includes a flat mounting flange with holes for the mounting hardware to attach to the aircraft. The housing is a relatively flat teardrop shape with a small cylinder toward the forward end of the housing to provide a radome for the antenna. The entire microwave package with the input connectors and the antenna completely assembled to the metal mounting plate fits into the open face of the housing. Pins on the housing are fit through holes in the mounting plate and the two parts heat-sealed together as a permanent assembly. An elastomeric mounting gasket is considered part of an installation kit to match the shape of the housing flange and to follow the contour of the particular aircraft involved, so that the installed microwave package is sealed to the aircraft outer skin.

AEL has considered several thermoplastic materials for this molded housing which appear to be compatible with the overall requirements, both electrical and mechanical; namely, polyethylene resin, ABS high heat resin, and Noryl phenylene oxide-based resin. Thermosetting resins were not considered because they are more expensive, both in raw material cost and also in unit molding costs.

AEL recommends using the ABS high heat resin, since its properties meet the needs of this requirement and since it is priced somewhat lower than Noryl. ABS high heat resin is being used in large quantities for components in the transportation field, and is therefore regularly processed by molders. Noryl has better thermal properties than ABS, but AEL does not feel the added cost of the final part can justify a higher-temperature-rated material when it is not warranted considering the ambient temperatures. Polyethylene was ruled out because the operating temperature range is too close to the maximum ambient to be worth risking thermal distortion for a relatively small savings in cost.

Environmental integrity. - Since the entire housing and radome assembly is a one-piece molded component, the design provides maximum environmental integrity. The ABS material selected is used in many applications for the transportation industry where severe environmental conditions such as rain, ice, detergents, sun, and temperature extremes must be withstood for a long period of time. In addition, it must withstand physical abuse. Based on these facts, AEL feels the proposed design will provide adequate environmental protection and integrity.

DESCRIPTION OF PROTOTYPE RF HEADS

This section describes the microwave RF heads, as built by AEL.

Bonded Stripline Front End Subassembly

Material. - Assemblies of the microwave bonded stripline front end in both K-6098 GT material and Duroid 5880 were assembled and tested during this development.

The tests of the K-6098 assemblies indicated that the RF filter in each board had a passband that varied by as much as 25 MHz from board-to-board. The source of passband variation from board-to-board was found to be the inconsistency of the dielectric constant in the K-6098 GT material. This inconsistency is highly undesirable, because it could result in a poor yield in production.

The packages of the bonded stripline front end in Duroid 5880 material were also tested and revealed to be highly consistent in all parameters.

The stripline package of K-6098 GT was therefore discarded in favor of using Duroid 5880 material. The tight dielectric control of the Duroid 5880 material ($E_r = 2.2 \pm .04$) will yield consistent performance from board-to-board in production. This represents a variation of about ± 1.82% in dielectric constant, which relates to an equivalent frequency shift of $\pm 3.3 \times 10^{-4}$ or about ± 1.68 MHz at C-band. An internal photograph of the stripline assembly is shown in Figure 22.

Stripline circuit performance. - The following results were obtained; using Duroid material:

Results	Goals
RF Bandpass Filter (Figure 22)	
Type = 5 pole, 0.5 dB ripple with 4.6% bandwidth	1.2% min.
Insertion Loss: 3.5 dB, Nom.	3.0 dB
4.93 GHz Rejection: 27 dB	40 dB
L.O. Bandpass Filter	
Type = 4 pole, 0.5 dB ripple with 8.2% bandwidth	1.3% min.
Insertion Loss: 1.5 dB, Nom.	1.5 dB
4.316 GHz Rejection: 37.5 dB	50 dB
5.482 GHz Rejection: 43 dB	50 dB
Test Coupler	
Insertion Loss: 0.21 dB	0.25 dB
Coupling: 21.5 dB	20 dB
Reverse Coupling (Isolation): > 32 dB	30 dB
Input-Output Return Loss: > 24 dB	20 dB
Coupled Port Return Loss: 11 dB	20 dB
Mixer	
LO Input: +2 dBm @ 4.9 GHz	+7 dBm
Conversion Loss: 6.4 dB	7 dB
LO Rejection at RF Port: 4.8 dB	15 dB
2 x 2 Rejection at -30 dBm RF: 57.4 dB	50 dB

These individual components were integrated for processing on a single substrate.

Microwave LO Source

The LO Amplifier Multiplier Assembly consists of a 305 MHz Class A amplifier, a X2 amplifier-multiplier and a X8 multiplier. An integrated assembly schematic diagram is shown in Figure 23.

Performance data for the components of the LO amplifier/multiplier chain is listed in Table 3.

The multiplier and IF circuits operate from a +15V DC supply which is applied to the RF head through the LO input connector. A 306 MHz LO input signal at a level of 0 dBm provided a +2 dBm output signal to the mixer at 4.896 GHz.

The configuration of the PC board design of the LO source and IF amplifier assembly is shown in Figure 24. The material used for the printed circuit board is G-10. The printed circuit board contains components of the 306 MHz Class A amplifier, the amplifier doubler, the X8 multiplier assembly and the IF amplifier. The X8 multiplier which increases the frequency from 612 to 4896 MHz is built as a subassembly solder mounted to the PC board. The X8 multiplier assembly is constructed on a brass plate which provides an improved ground plane. The output resonator is mounted into the ground plane as an integral part of the assembly. The brass assembly type of construction minimizes the ground path inductance in the 4.9 GHz output circuit which could otherwise cause circuit instability and lack of repeatably good electrical performance.

<u>Amplifier-multiplier design details</u>. - The 306 MHz amplifier (Q1) is designed using an NE73432 California Eastern Labs transistor. The transistor is operated in the common emitter, Class A mode of operation. The circuit has a minimum gain of 12 dB over the 304 to 308 MHz frequency range. The circuit is designed to operate at an input power level of 0 $\pm$3 dBm and has a worst case input VSWR of 1.4:1.

The amplifier was shown schematically in Figure 23. Resistors R3 and R4 provide proper transistor quiescent operating point. Capacitors C11 and C12 provide decoupling for RF chokes L4 and L5. Components C10 and L3 match the transistor input impedance to 50 ohms and C9 provides a DC block at the input. L6 and C13 provide a part of the interstage matching circuit between Q2 and Q3.

The amplifier-doubler (Q3) is designed using a 2N4428 transistor. The circuit provides a minimum of 4 dB gain for a 608 to 616 MHz 2nd harmonic output frequency when the fundamental input is 304 to 308 MHz. The fundamental and third harmonic outputs of the amplifier-doubler are a minimum of 25 dB down from the second harmonic. The minimum input VSWR is 1.2:1.

The amplifier-doubler is also shown schematically in Figure 23. The amplifier section of the circuit operates in the Class C, common emitter mode of operation. The amplifier is capable of providing approximately 11 dB gain at the fundamental with a collector efficiency of 55%. The matching network of L11 and C20 resonate with the

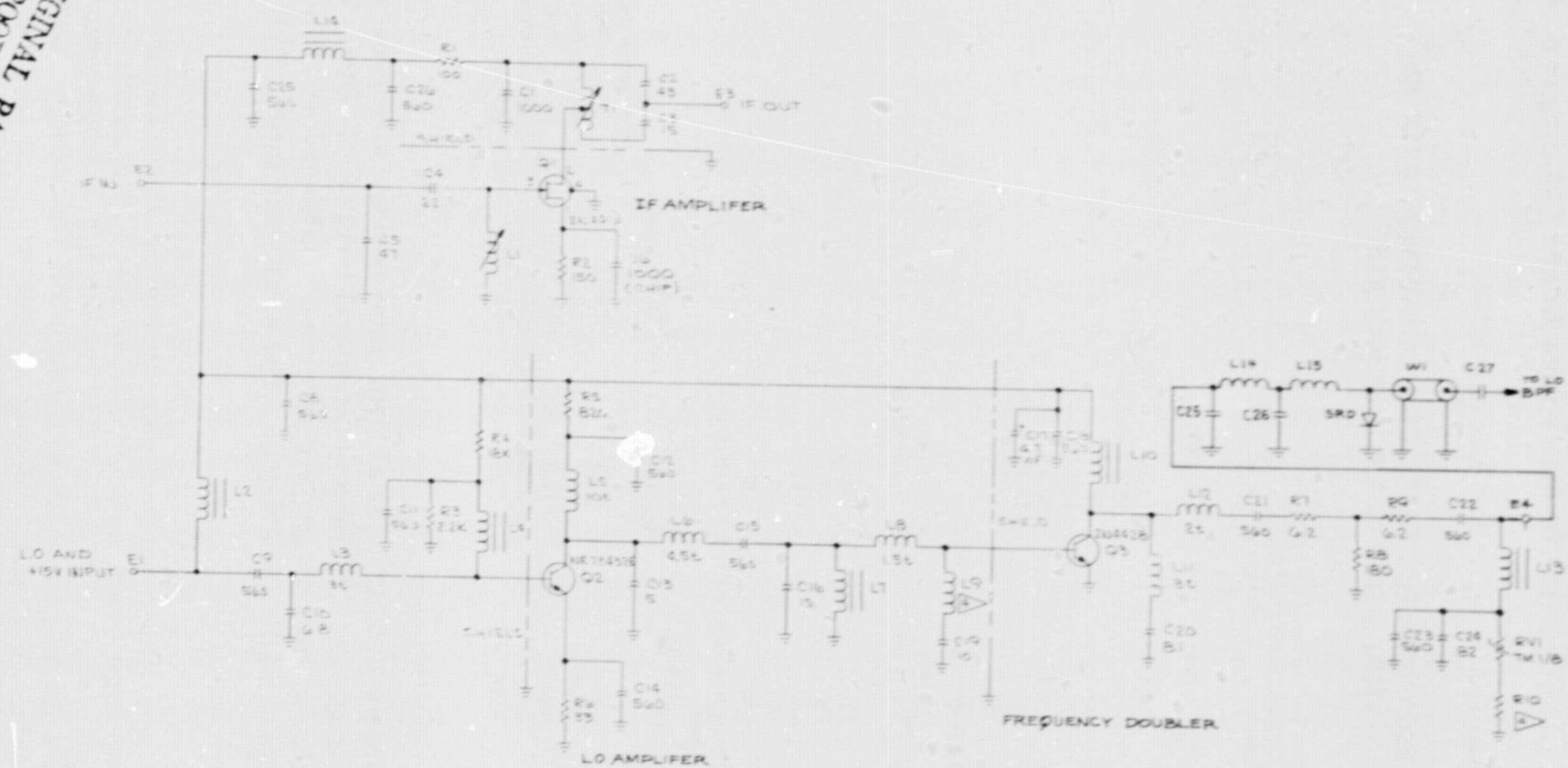


FIGURE 23. SCHEMATIC DIAGRAM, LO AMP/MULTIPLIER AND IF

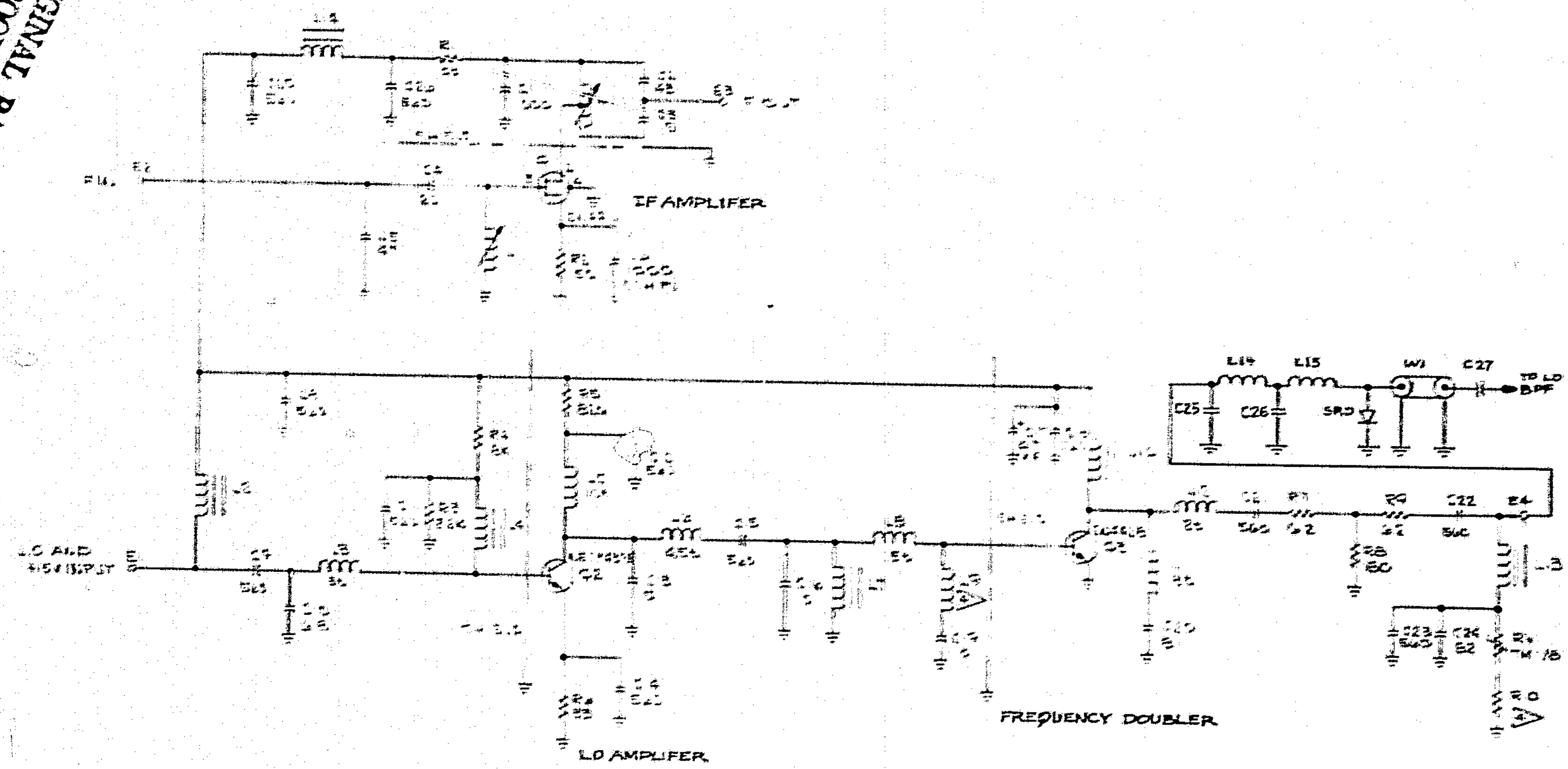


FIGURE 23. SCHEMATIC DIAGRAM, LO AMP/MULTIPLIER AND IF

transistor output impedance at the fundamental frequency and encourage second harmonic generation. The idler circuit of L9 and C19 provide a return path of the 2nd harmonic currents in the transistor input circuit. The components L7 and C16, are part of the interstage matching circuit for Q2 and Q3. Inductance L12 matches the multiplier output impedance to 50 ohms and C21 is a DC blocking capacitor.

TABLE 3. PERFORMANCE DATA FOR COMPONENTS OF THE LO AMPLIFIER MULTIPLIER CHAIN

306 MHZ AMPLIFIER DATA
f_{in} = 306 MHz V_{cc} = 15 VOLTS

P_{in} (dBm)	P_{out} (dBm)	GAIN (dB)
−3	+10.4	13.4
−2	+11.4	13.4
−1	+13.1	14.1
0	+13.5	13.5
1	+13.7	12.7
2	+14.3	12.3
3	+14.7	11.7

DOUBLER AMPLIFIER DATA

P_{in} (dBm) (f_{in} = 306 MHz)	P_{out} (dBm) (2 f_{in} = 612 MHz)	P_{out} (dBm) (3 f_{in} = 918 MHz)
+10	+14	−8
+11	+15	−8
+12	+16	−7
+13	+17	−5
+14	+18	0

X8 MULTIPLIER CONVERSION LOSS VS. FREQUENCY
(P_{in} = 15 dBm)

f_{in} (MHz)	f_{out} (MHz)	Conv.* loss (dB)	P_{out} (P_{in} = +15 dBm)
608	4864	11.4	+3.6
610	4880	11.1	+3.9
612	4896	10.9	+4.1
614	4912	11.0	+4.0
616	4928	11.1	+3.9

*Conversion loss. These conversion loss numbers include 2 dB of filter insertion loss.

The X8 multiplier is designed using an axial lead, glass package step recovery diode. The circuit is designed to operate at an input signal level of +15 dBm. The conversion loss of the multiplier is 8 dB and will provide a +7 dBm output power level at 4.89 GHz with a +15 dBm 612 MHz input signal. The worst case input VSWR of the circuit is 1.7:1.

The X8 multiplier is also shown schematically in Figure 23. The circuits consist of an axial lead, glass package diode mounted across a 4.9 GHz quarter wave stripline resonator (W1). The idler circuit of L15 and C26 are energy storage components which charge the resonator once during each cycle of the input frequency. Components L14 and C25 provide input matching at the fundamental frequency. A bias network is

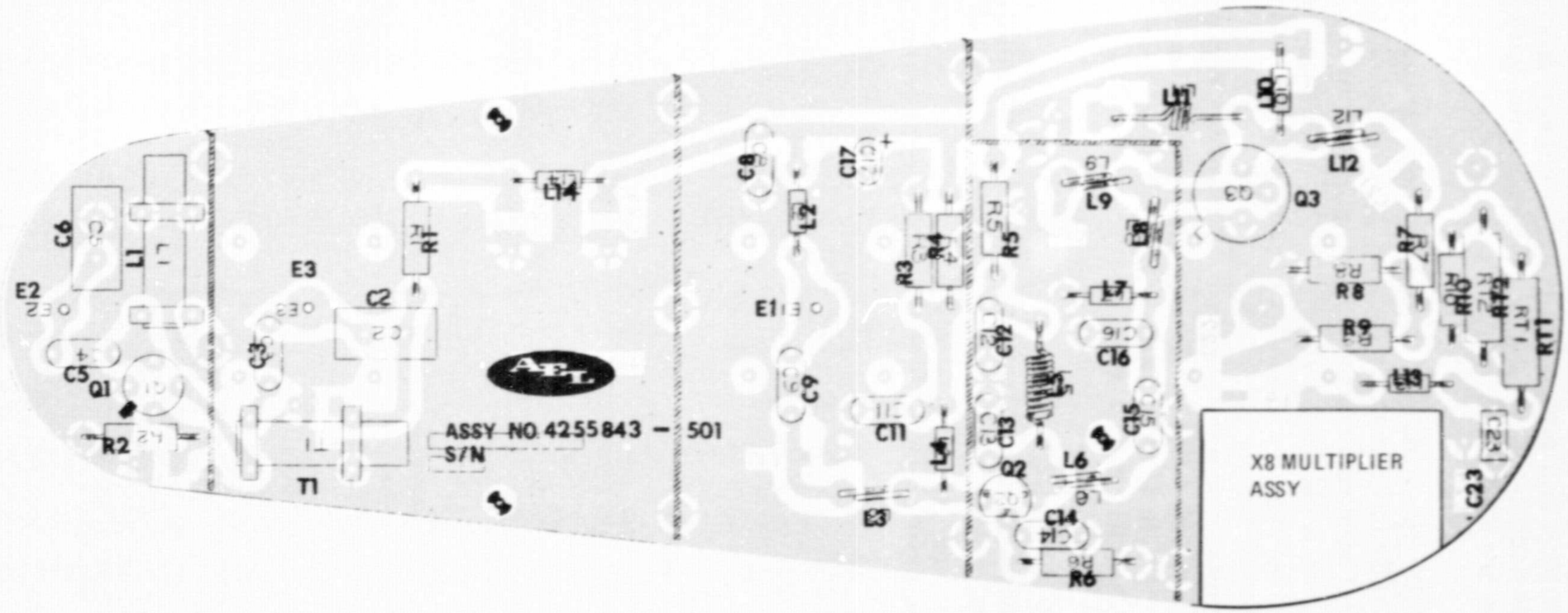


FIGURE 24. BOARD ASSEMBLY, LO AMP/MULTIPLIER

composed of L13, R10, C23 and C24. C27 couples energy from the transformer W1 into the L.O. bandpass filter. Transformer W1 resonates with the undesirable parasitics of the glass package diode.

Matching instabilities. - Initial integration problems were noted when the X8 multiplier would not stabily interface with the amplifier doubler. Investigation showed that there were low level harmonics of the X8 multiplier output present at the input. To overcome the harmonic problem at the lowest cost, a TEE pad consisting of R7, R8 and R9 was installed between the amplifier doubler and X8 multiplier.

Amplifier/multiplier assembly package. - Figures 25 and 26 show the amplifier multiplier assembly, complete with shields and SRD cavity.

Integrated RF Head Packaging

Figure 27 shows the integrated microwave assembly, edge view, showing antenna elements and LO connection.

Figure 28 shows the top view of the cylindrical antenna version of the radome of the RF head.

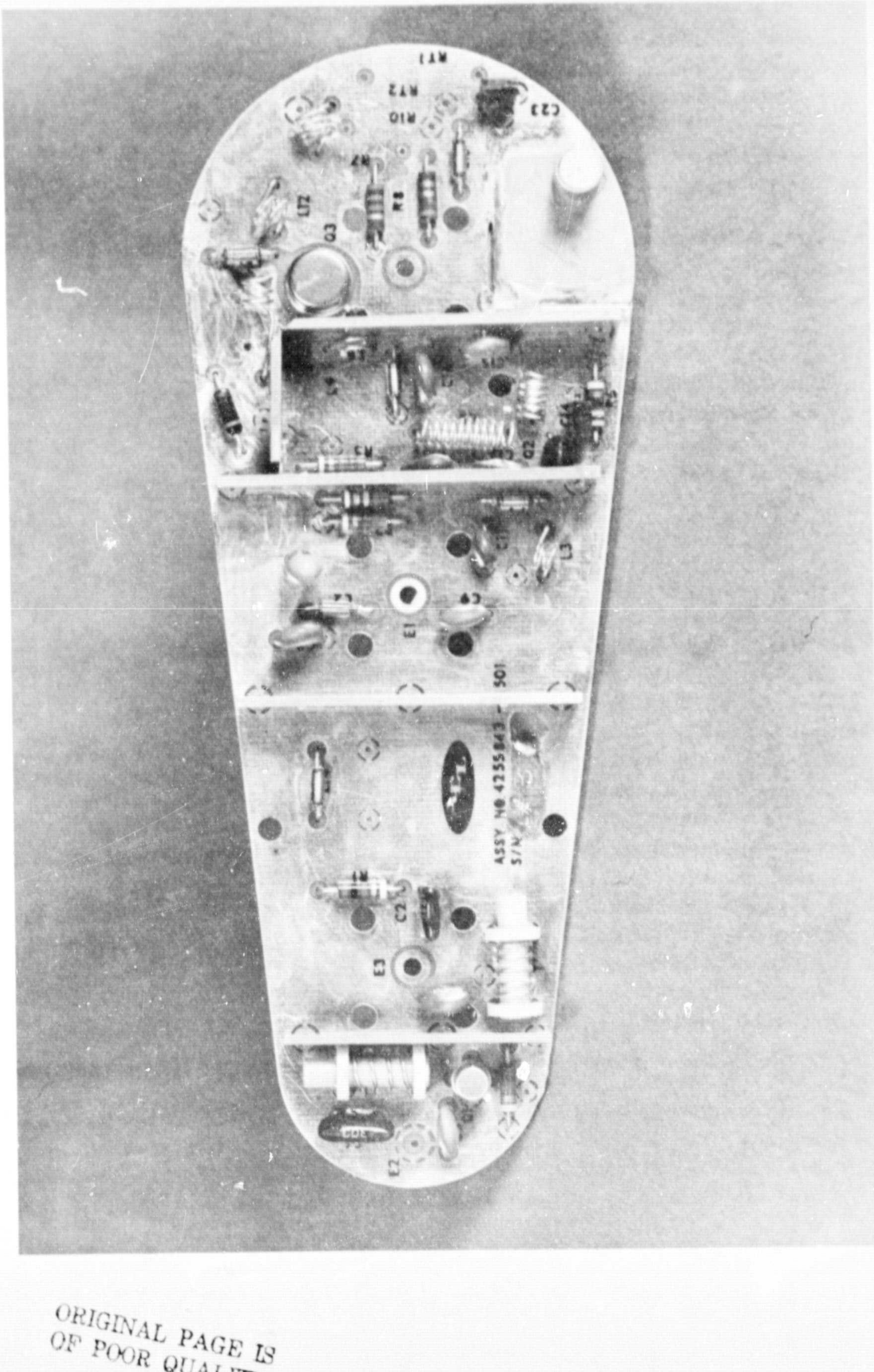


FIGURE 25. MICROWAVE MULTIPLIER ASSY, TOP VIEW

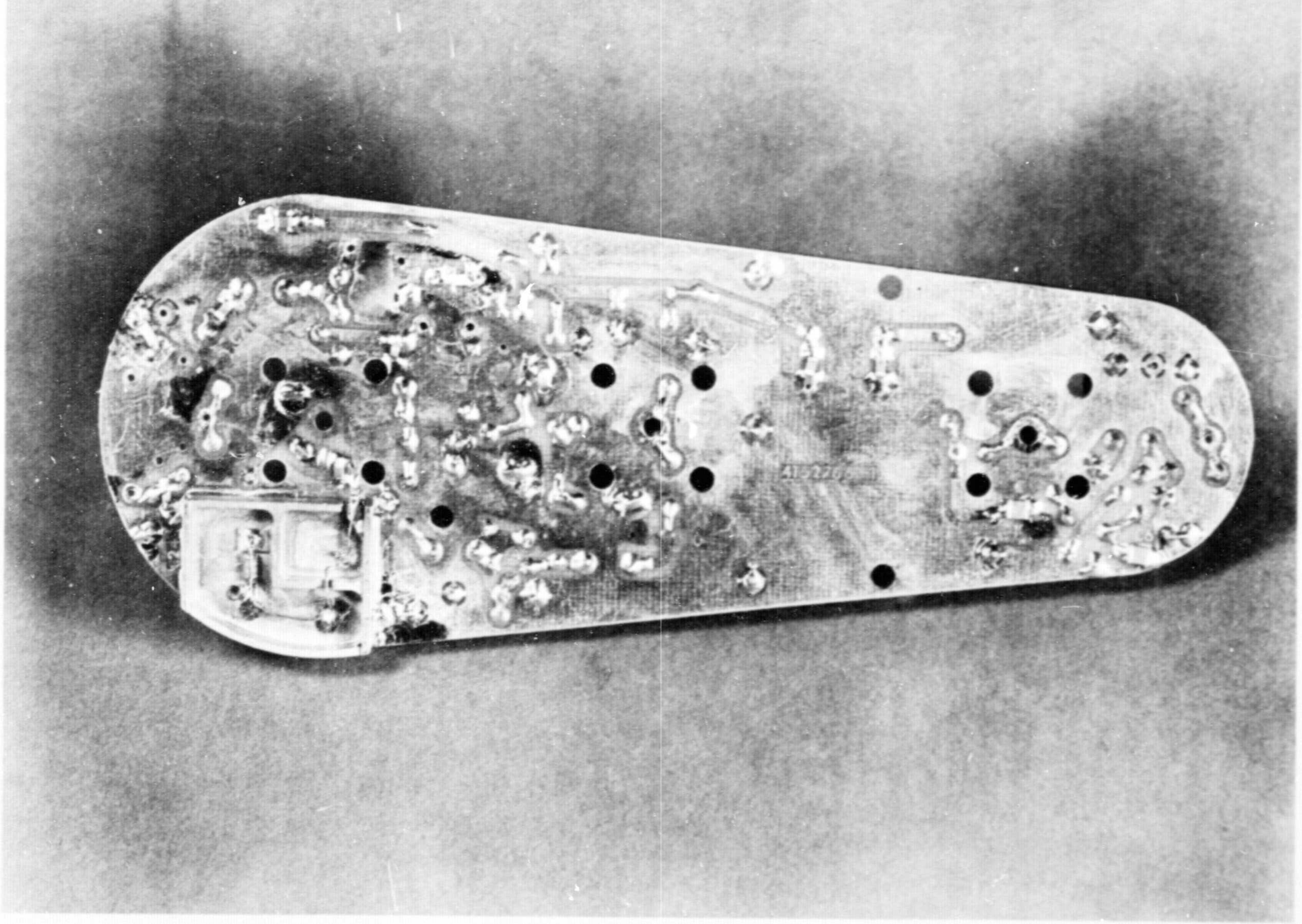


FIGURE 26. MICROWAVE MULTIPLIER ASSY, BOTTOM VIEW

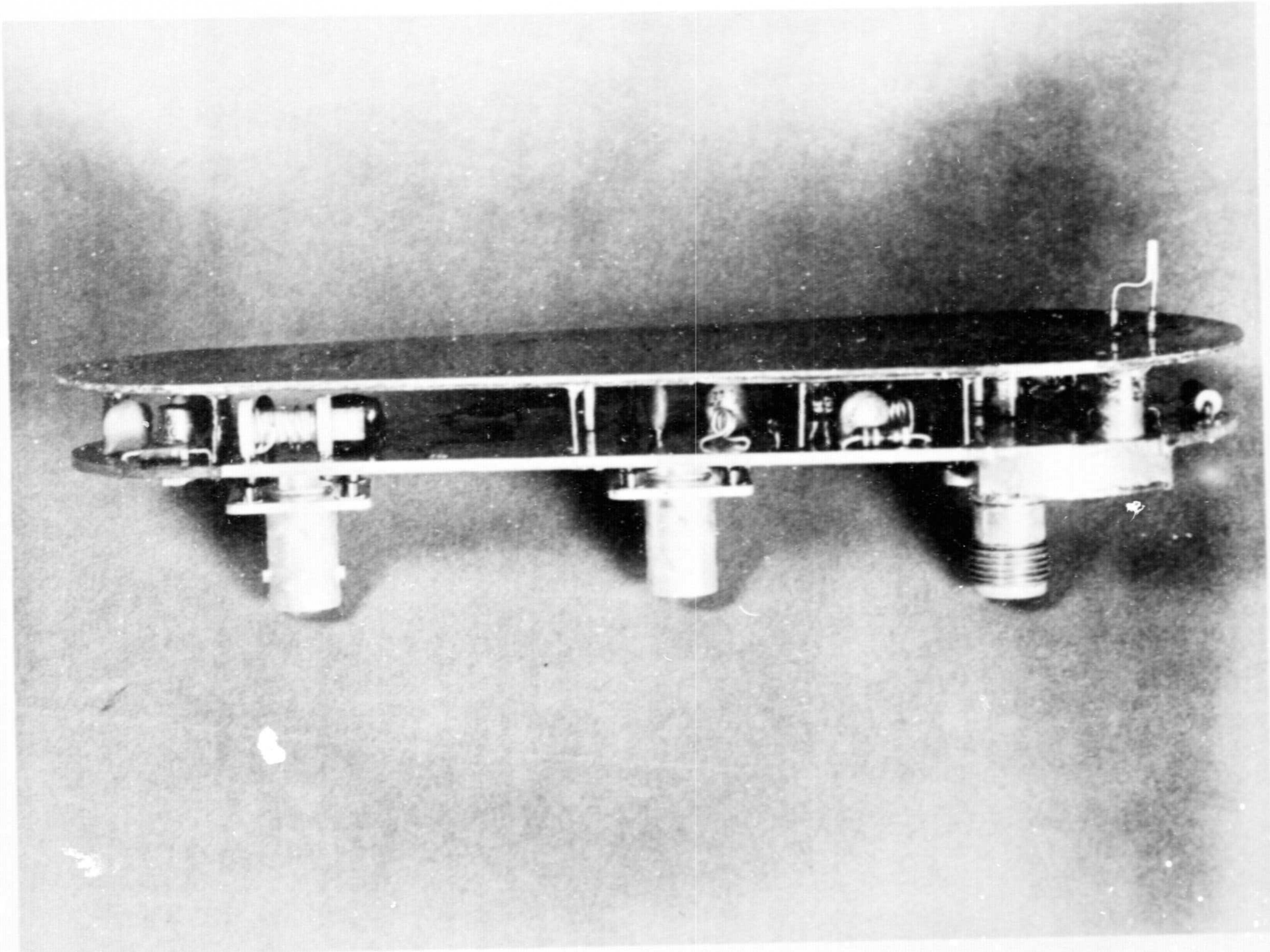


FIGURE 27. INTEGRATED MICROWAVE ASSEMBLY

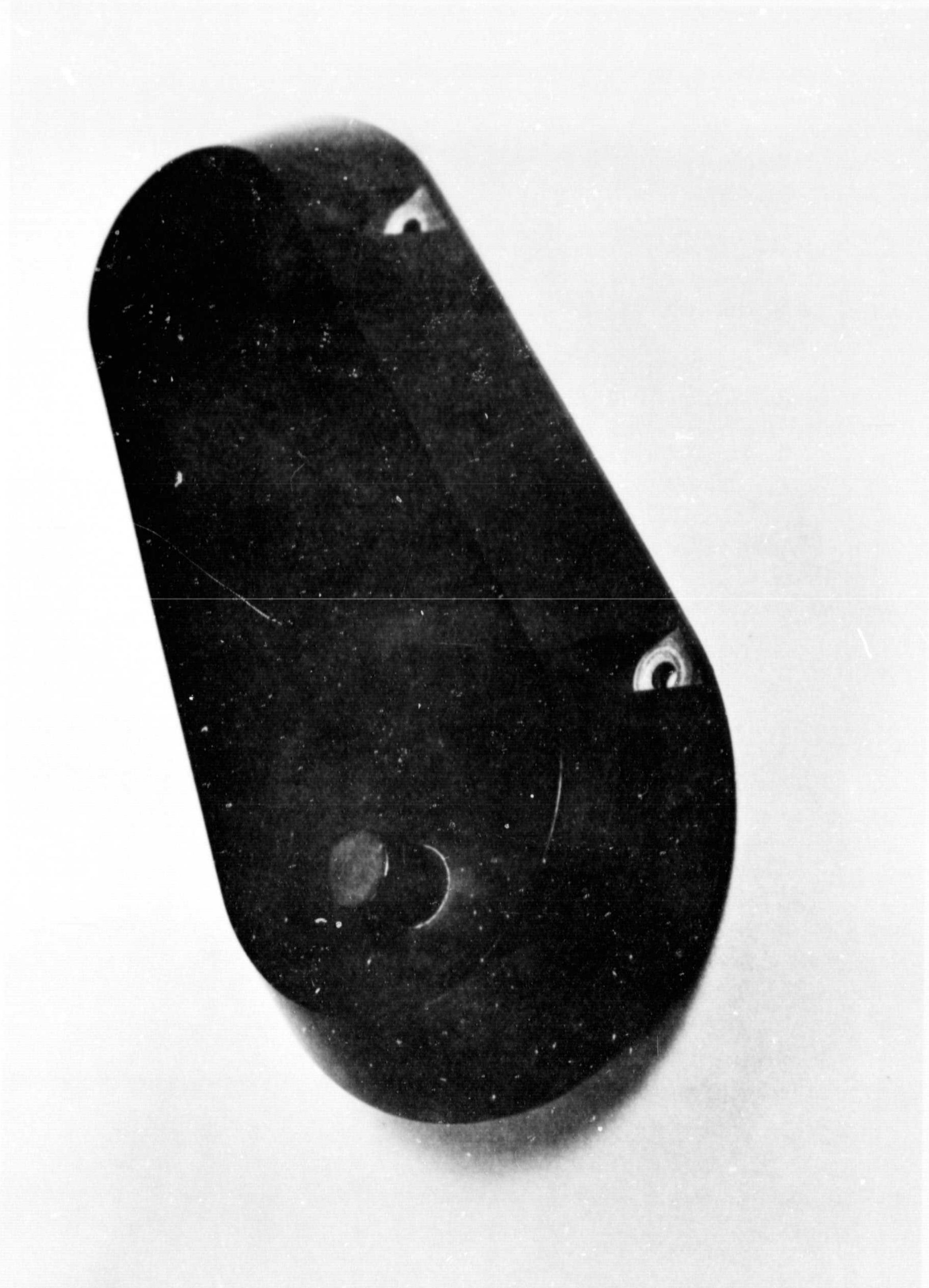


FIGURE 28. TOP VIEW, RF HEAD

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SYNTHESIZER ASSEMBLY

The frequency synthesizer for the Low Cost MLS Receiver has been integrated onto one printed wiring board assembly, consisting of the following individual circuits:

1. Reference Oscillator
2. Loop Phase Detector and Filter
3. VCO and Divide-by-2 Prescaler
4. Mixer/Shaper
5. Divide-by-N Counter
6. Switch Decoder
7. X125 Multiplier

The synthesizer is of the offset type, and the block diagram is shown in Figure 29.

The offset synthesizer is so named due to the 150 MHz offset introduced into the feedback loop. This translation reduces the magnitude of division ($\div$N) required to reach the reference frequency of 9.375 kHz. In this model, N is constrained between 234 and 433 with an input frequency of 2.19375 MHz to 4.059375 MHz. Given these parameters, several choices of components are available to make up the $\div$N function, such as the single chip programmable divider elements produced by Hughes (HCTP0320P) and RCA (CD4059). In both cases, however, the devices are single source items and can be replaced by multiple packages of conventional TTL elements at lower cost. The single most important advantage of this type synthesizer is the low divide-by-N ratio which results in less DC gain required after the phase detector and improved synthesizer sideband noise performance over models with higher divide-by-N ratios.

The reference oscillator provides 4.8 MHz to a ripple counter which delivers a 9.375 kHz reference to the synthesizer loop phase detector and a 1.2 MHz reference to the 150 MHz phase locked oscillator. The temperature stability of the reference oscillator is nominally 0.00125 percent which is achievable without oven stabilization but will place tighter constraints on the 10.8 MHz LF filtering. The tradeoff factors involved in this choice of stability versus IF bandwidth are presented in the IF/Detectors discussion of this report.

The second local oscillator injection frequency of 150 MHz can be alternately developed in a phase locked loop composed of a MC1648 VCO, MC4044 phase detector, and MC12000 multiplying mixer to offset the 150 MHz VCO to 1.2 MHz for comparison at the phase detector.

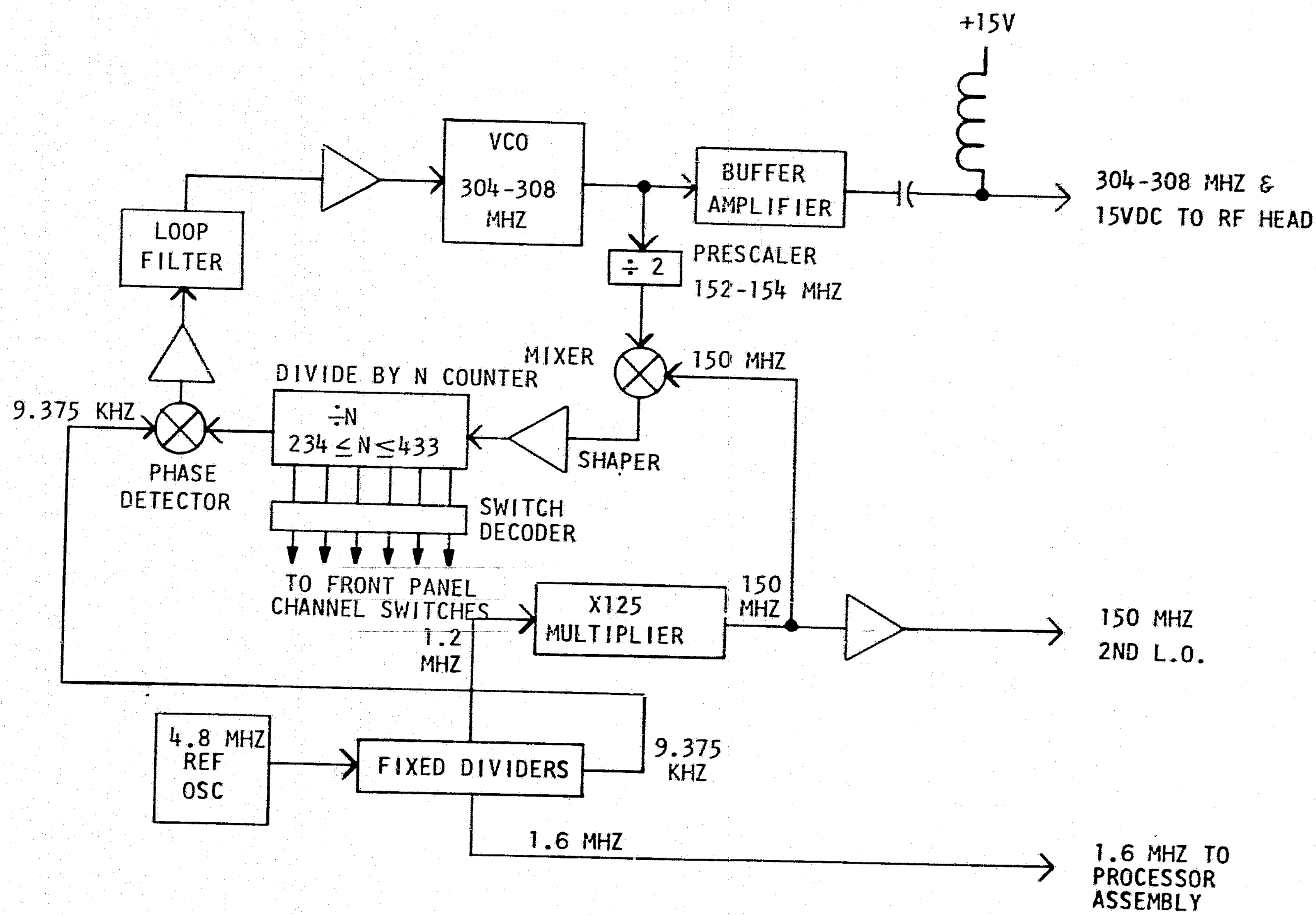


FIGURE 29. LCMLS SYNTHESIZER BLOCK DIAGRAM

Synthesizer Circuits

The reference oscillator schematic is included in Figure 30 and uses a 2N3662 in a modified Colpitts circuit with the crystal also serving as a series resonant filter for the output. Temperature tests on this oscillator show ± 10 ppm performance of +65°C to -15°C. The goal established during Task 1 for this parameter was ± 15 ppm. A ripple binary counter U_1 provides 1.2 MHz and 9.875 kHz signals for use in the X125 multiplier and loop phase detector respectively.

Figure 30 also shows the Divide-by-N counter, switch buffers and switch decoding circuitry used to preset the Divide-by-N counter. The divide-by-N counter is made up of three 74LS192 counters which divide the 2-4 MHz input to a 9.875 kHz output. This occurs as N is varied from 234 to 433. The programmed count is derived from the channel select switches which provide a BCD output from 000 to 199. These numbers are offset by 234 in the decoding circuit.

The schematic of the X125 Multiplier is also shown in Figure 30. This multiplier technique was chosen as a cost effective approach to generating the 150 MHz used for the second LO and the synthesizer offset. The multiplier is essentially three linear gain stages with interstage diode clipping to generate harmonics. Because of the linear nature of the stages, alignment is straightforward and fast.

The loop filter schematic is included in Figure 30. Integrated circuit U11 is a J-FET input dual 741 op-amp possessing very low input bias current levels and exceptionally high input impedance. The filter provides a D. C. gain of 120 with the first low pass corner at nominally 50 Hz. The synthesizer output spectrum shows the 9.875 kHz sidebands to be suppressed 60 dB.

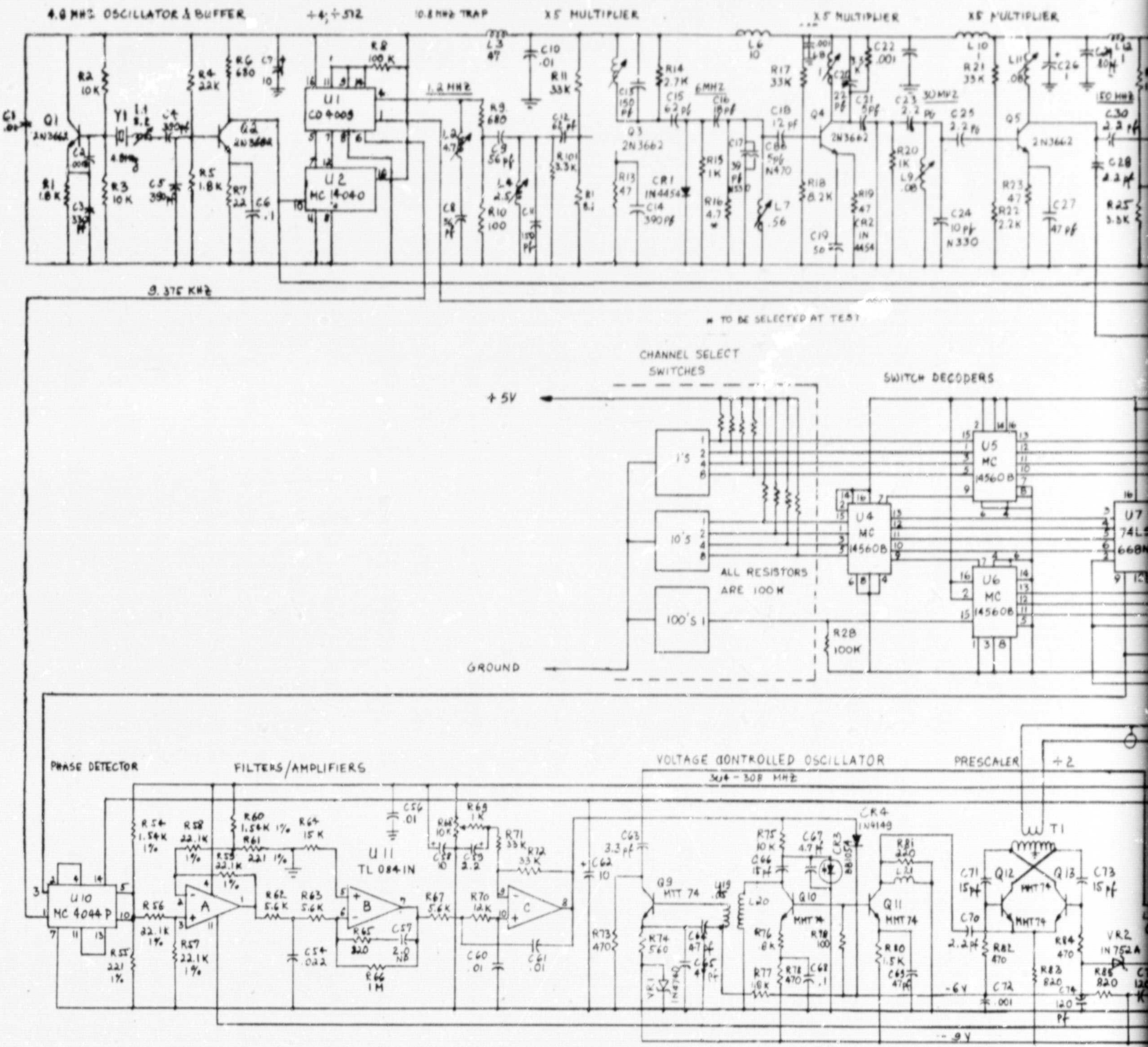
The schematic of the VCO and divide-by-2 pre-scaler is included in Figure 30. This circuit is nearly identical to the synthesizer of the Narco DME-190. Capacitors C66 and C67 were added to reduce the sensitivity of the VCO from 12 MHz/volt to 1 MHz/volt and thereby a 20 dB improvement in incidental FM.

The circuit of the mixer/shaper is included in Figure 30. The mixer uses a dual gate FET to translate the 152-154 MHz from the pre-scaler to the 2 to 4 MHz band. The 150 MHz used in translation is the same signal used for the second conversion to 10.8 MHz in the IF. The 2N3662 following the mixer is a saturating amplifier which squares up the mixer output and adjusts the level for the TTL dividers.

Synthesizer Construction

The assembly drawing for the MLS synthesizer is shown in Figure 31. Due to the addition of eggcrate shielding; it was decided to place certain resistors on the bottom side of the printed wiring card. This would not be done in production, since it is not compatible with automatic lead insertion and flow soldering hence would require hand soldering of these components.

Figures 32, 33, and 34 show photographs of the synthesizer assembly in enclosed, top and bottom views, respectively.



FOLDOUT FRAME

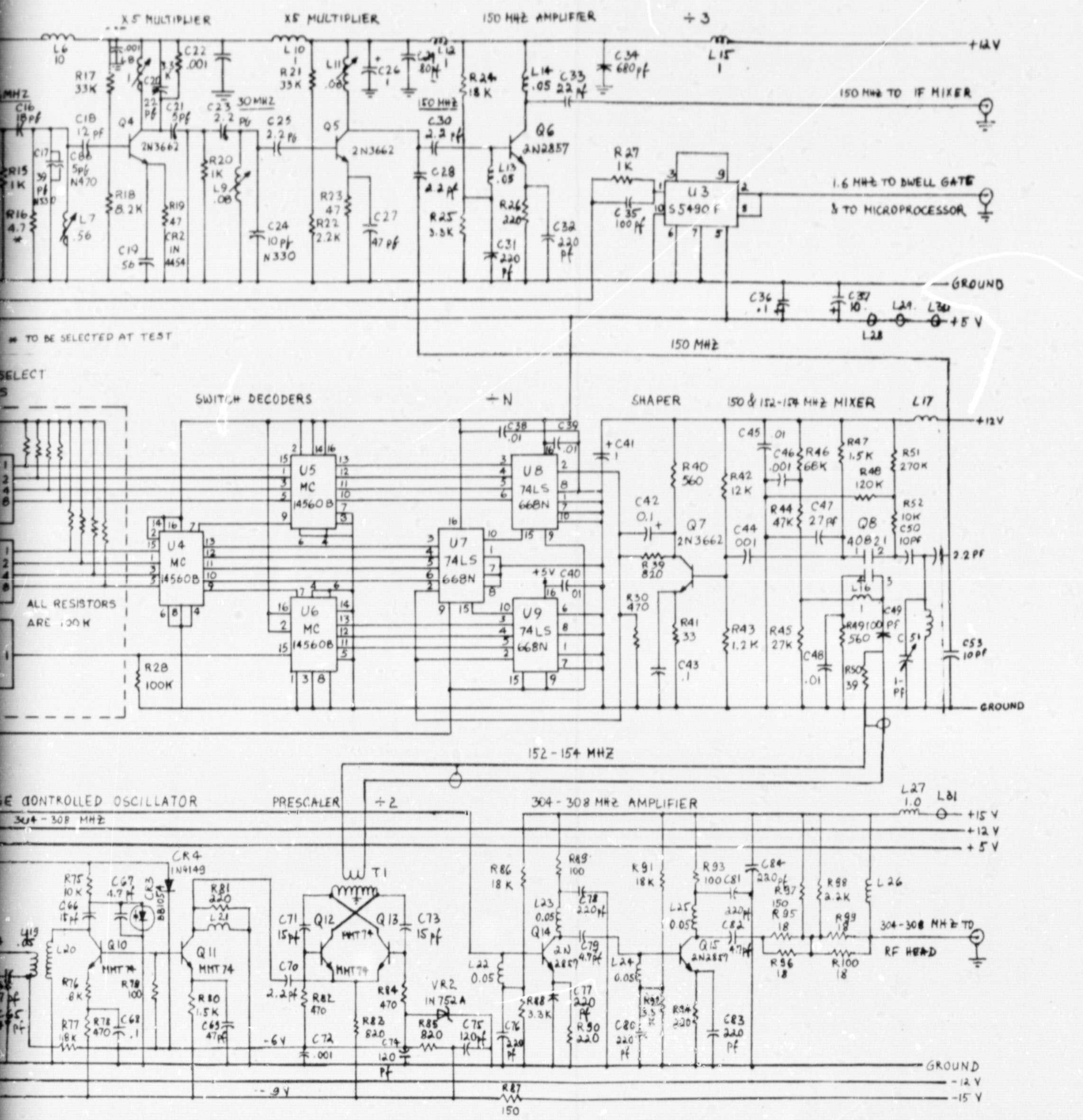
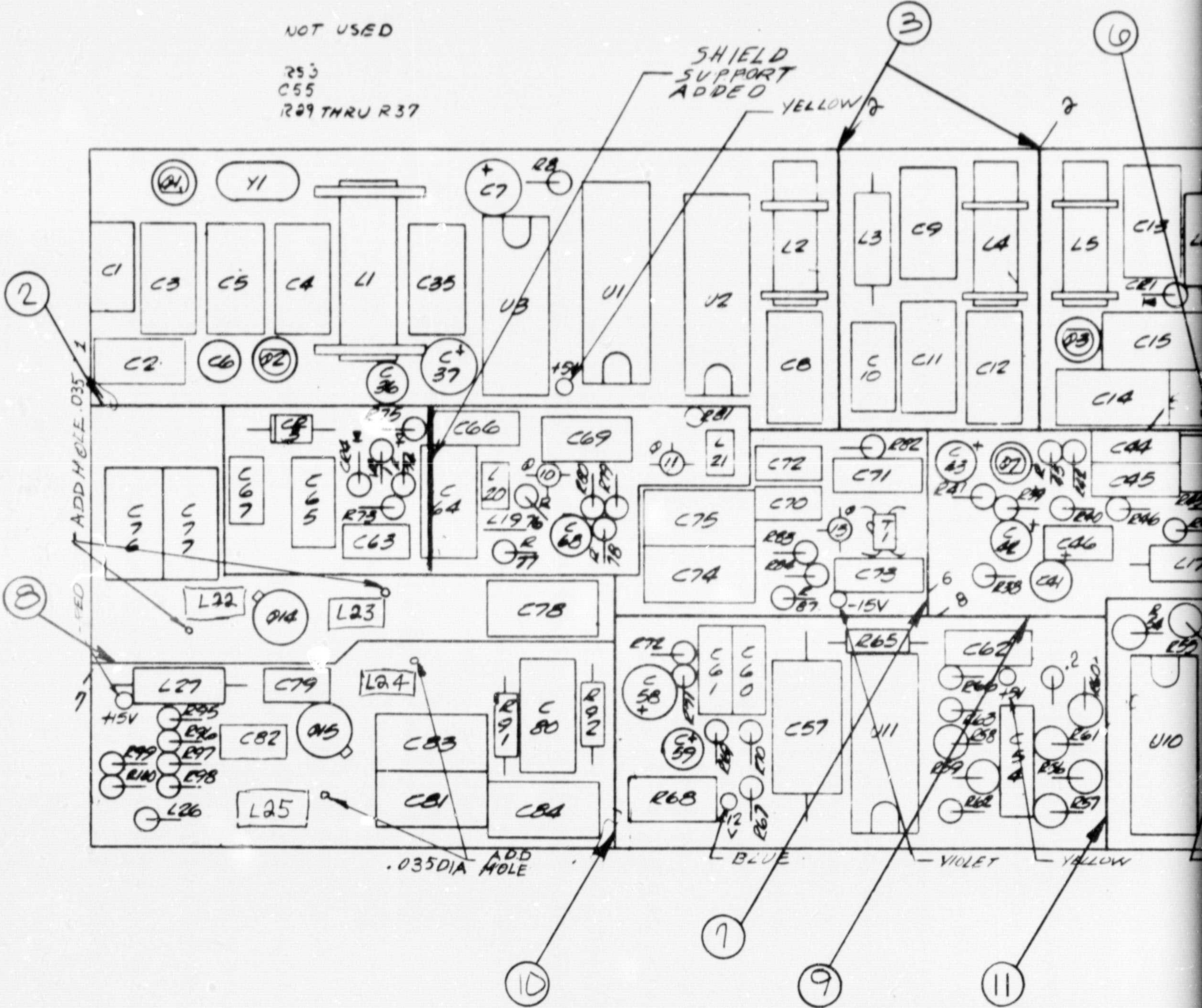


FIGURE 30. SCHEMATIC DIAGRAM
SYNTHESIZER

FOLDOUT FRAME 2

NOT USED

R53
C55
R29 THRU R37



FOLDOUT FRAME 1

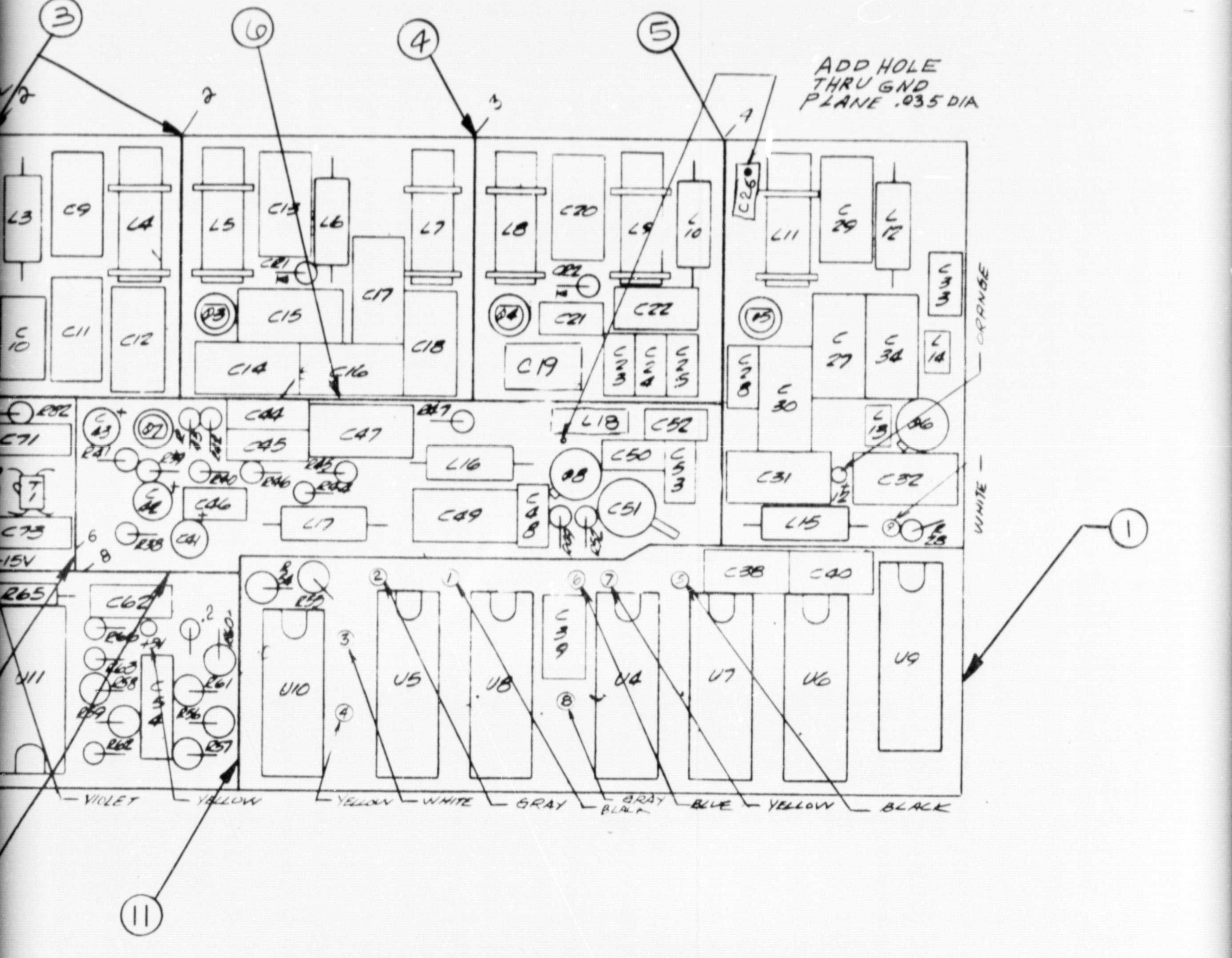


FIGURE 31. BOARD ASSEMBLY, SYNTHESIZER

FOLDOUT FRAME 2

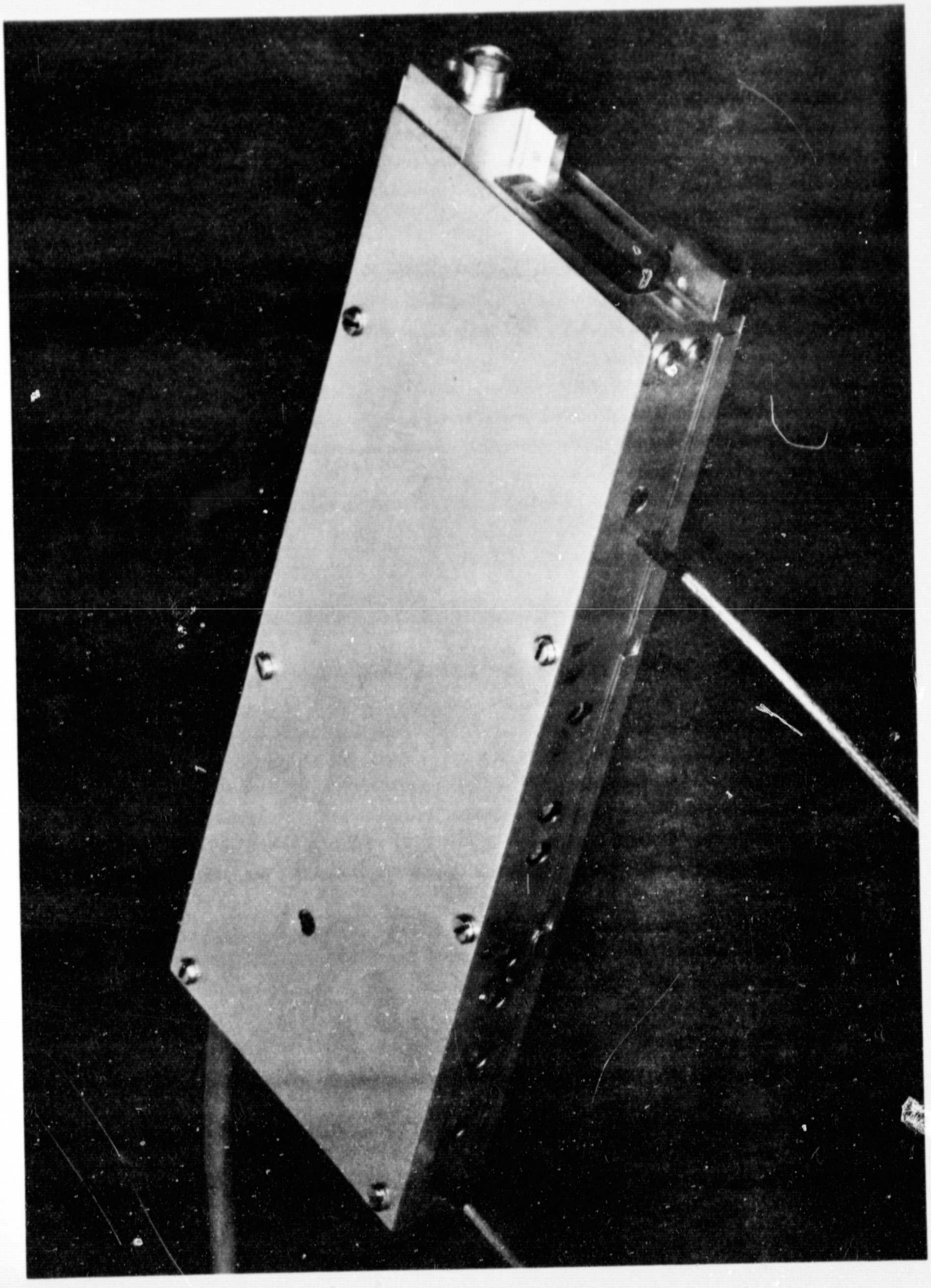


FIGURE 32. ENCLOSED SYNTHESIZER ASSEMBLY

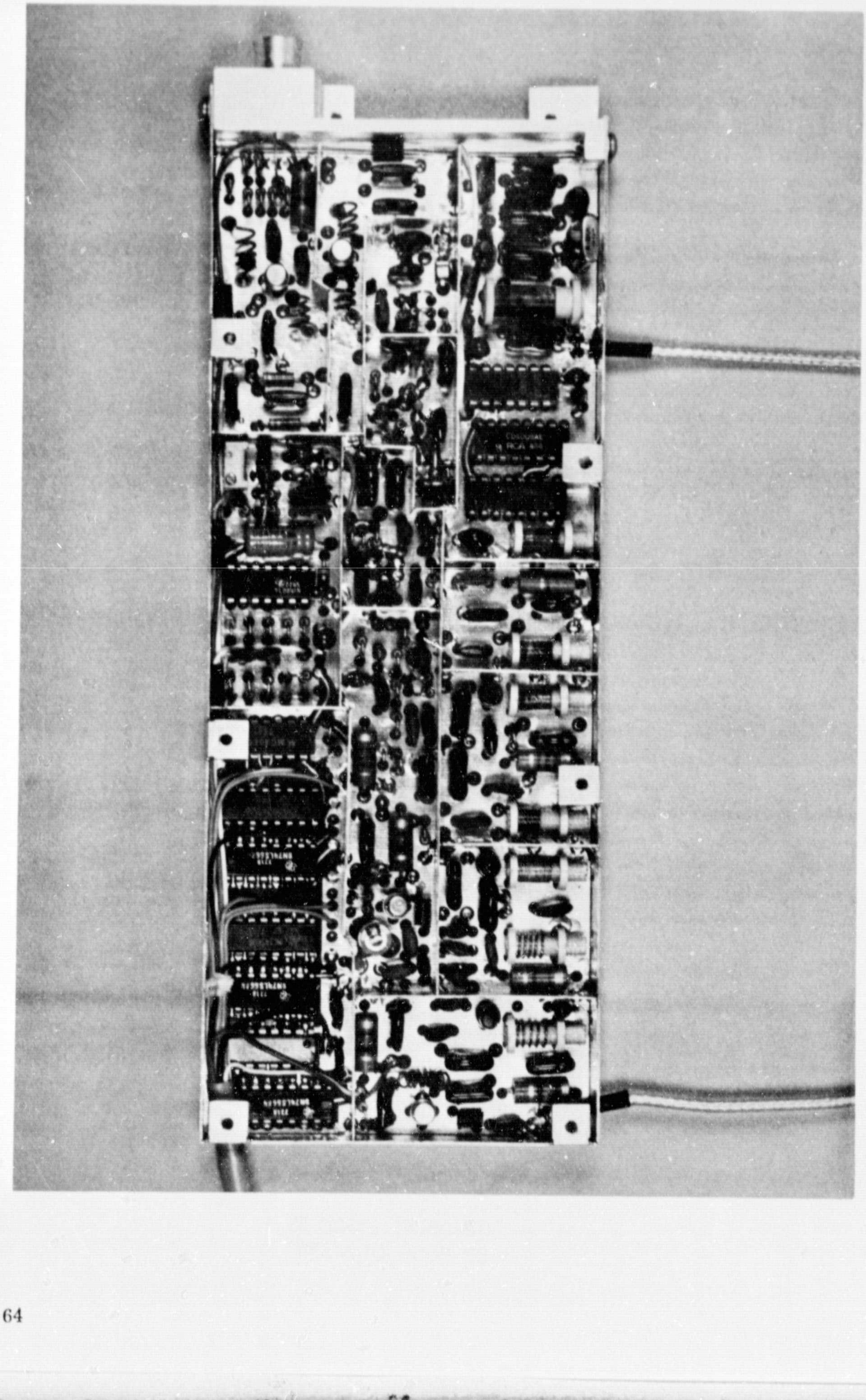


FIGURE 33. SYNTHESIZER TOP VIEW

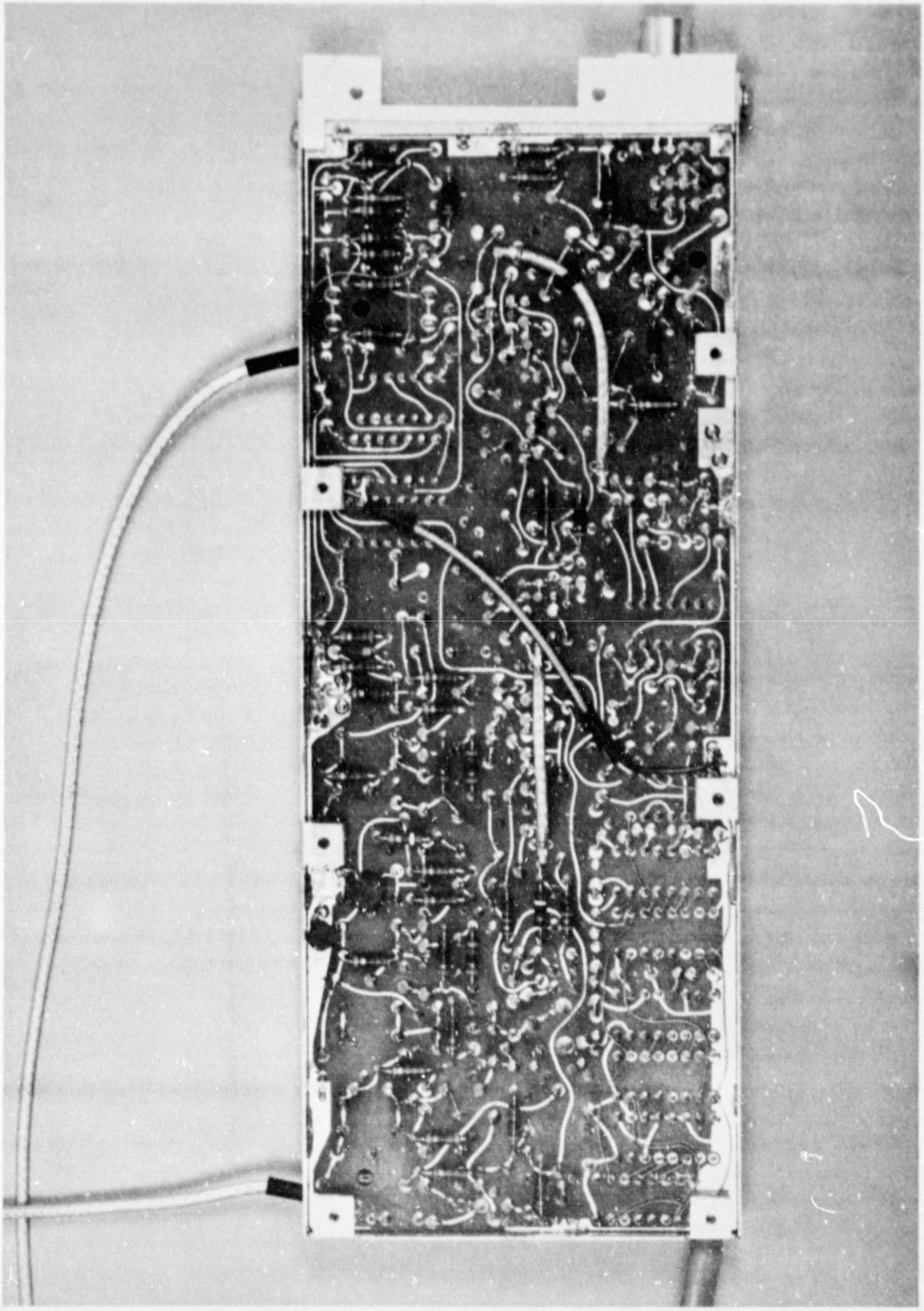


FIGURE 34. SYNTHESIZER BOTTOM VIEW

IF/DETECTOR SUBASSEMBLY

The IF/Detectors Subassembly consists of a single printed wiring card containing the following circuits:

1. 1st IF Amplifier and Filter
2. 2nd Mixer
3. 2nd IF Amplifier
4. 2nd IF Filter
5. Log IF for Video
6. FM Demodulator for DPSK

One of the fundamental design-to-price trade-offs occured when considering the effect of LO stability on the 2nd IF filter shape factor. It is necessary to provide about 50 dB of rejection to the adjacent channel at ±295 kHz from the desired channel; yet, the 3 dB bandwidth must be sufficient to pass the 60 kHz information bandwidth. If the master oscillator, hence receiver tuned frequency, was inaccurate by a tolerance of ± 0.001 percent, for example, then the receiver passband would have been opened by an additional ± 51 kHz (102 kHz) to a total of 162 kHz minimum.

In addition, the 2nd IF filter itself possesses an inherent center frequency tolerance. Since crystal filters are not cost effective at this bandwidth, LC filters were used, with an inherent center frequency tolerance of 0.015 percent at best, or ±15 kHz, which adds 30 kHz to the required 3 dB bandwidth. Thus the required 3 dB filter bandwidth becomes:

$$BW_{3\ dB} = \text{Information BW} + (\text{RF Freq})\ (\text{Osc. Tol}) + \text{IF CF Tol.}$$
$$= 60 + \underline{5.0 \times 10^6}\ (\text{Osc. Tol.}) + 30\ (\text{kHz})$$

However, the filter shape factor is:

$$SF = \frac{BW_{50\ dB}}{BW_{3\ dB}}$$ which is therefore inversely proportional to the master oscillator

stability. The cost of a filter in turn, is inversely proportional to the shape factor, according to the relationship described in Figure 35. Similarly, the cost of a crystal is inversely proportional to its tolerance, as also shown. Note the abrupt jump in crystal cost when an oven is required at 0.001 percent tolerance and below.

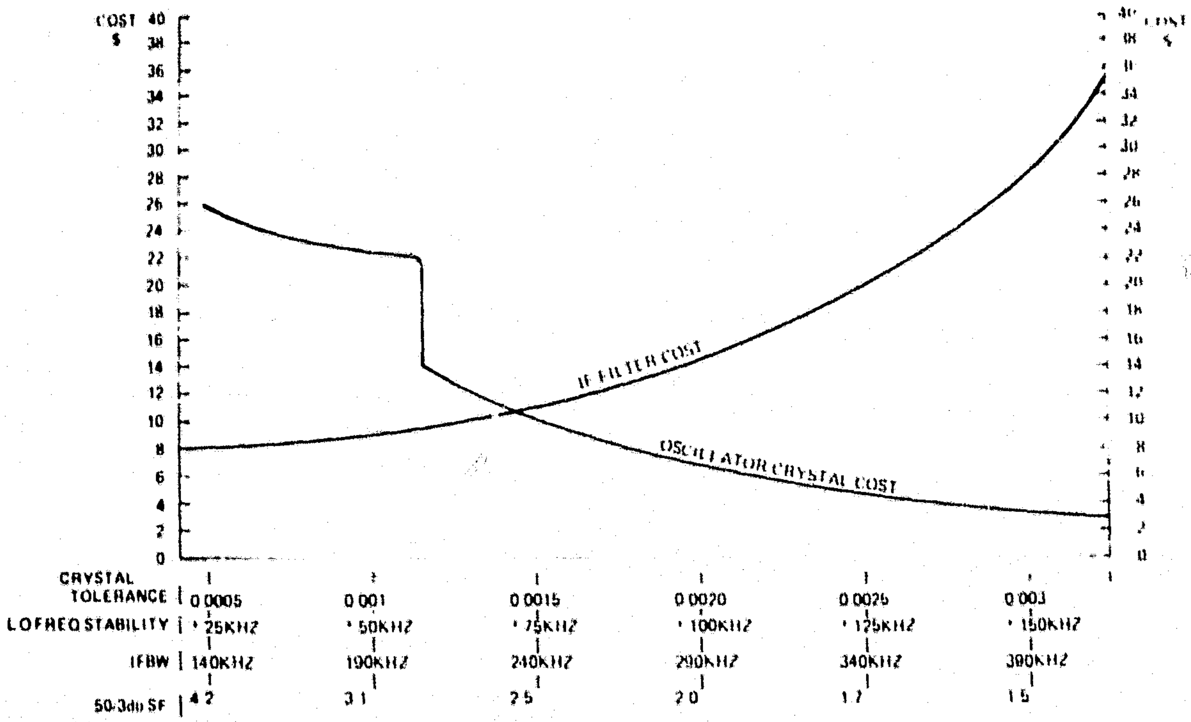


FIGURE 35. LOW COST MLS LO VERSUS IF FILTER TRADE-OFFS

Therefore, the minimum, hence optimum, total cost for the combination of filter and oscillator crystal, assuming that the possible 1.2 dB reduction in sensitivity due to a wider bandwidth can be temporarily set aside, is in the 0.00120 crystal tolerance/210 kHz filter bandwidth area.

Use of Surface Acoustic Wave (SAW) filters could possibly produce the required wide bandwidth at the 10.8 MHz frequency with better CF tolerance, but are definitely more expensive than LC designs at this time, and are more lossy, hence requiring additional gain stages.

Changes of 2nd IF frequency in order to optimize the filter is not recommended. A higher 2nd IF would not allow crystal filters (25 MHz maximum CF for a fundamental crystal but with about 75 kHz absolute maximum bandwidth) and would also preclude the choice of the CA3089 log IF/demodulator. A lower 2nd IF would create image problems that could only be solved by a more expensive 1st IF filter.

1st IF/2nd Mixer/2nd IF

A dual conversion IF chain was chosen for the MLS receiver since it allows performance requirements to be met with the minimum number of frequency conversions, hence, minimum number of components and cost. The first IF frequency of 160.8 MHz is sufficiently high such that image, spurious and LO signals are separated from the desired

frequencies such that these unwanted responses and emissions may be conveniently rejected by the RF preselector. The second IF frequency is sufficiently low to allow use of a multifunction IF integrated circuit and an LC filter. The ratio of the first to second IF frequencies is approximately 15:1, which is appropriate for rejection of the second image by straightforward first IF filtering. Since the previously listed filtering conditions can be met by the two IF frequencies chosen, a simpler and lower cost design results because fewer LO frequencies must be generated and fewer mixers and filters are required.

The circuitry required for the 1st IF/2nd Mixer/2nd IF was not considered a critical portion of the cost/performance trade-off. This is because this circuitry is not a high cost item and would therefore not be an efficient area of highly concentrated study, and because existing circuits are available which are highly similar and familiar to avionics equipment manufacturers.

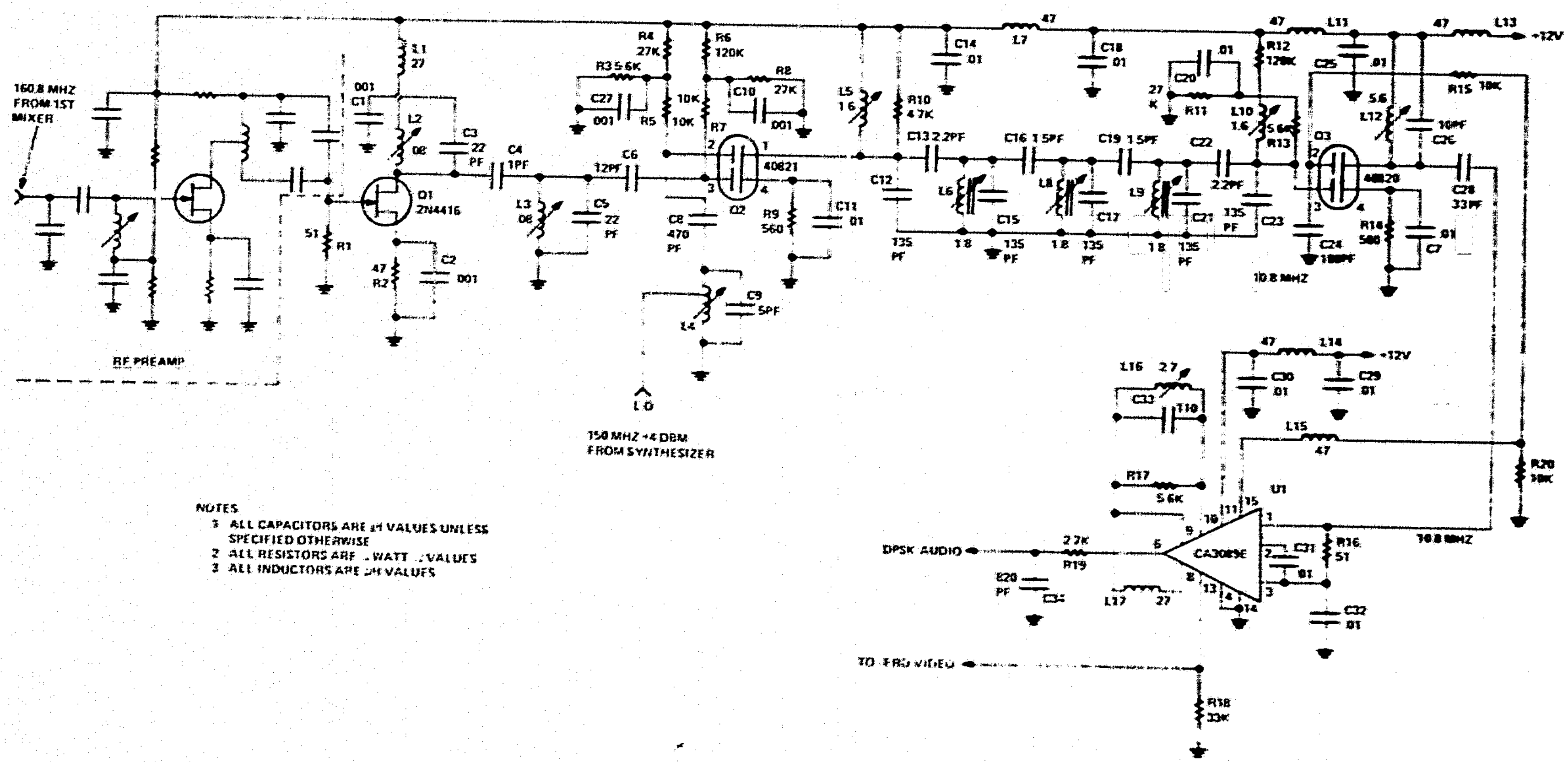
The 160.8 MHz First IF schematic diagram is shown in Figure 36 and is composed of two gain stages, a bandpass filter, and a 150 MHz trap. The first gain stage is located in the remote mounted RF head to provide gain and establish the receiver overall noise figure prior to the interconnecting coaxial cable. The active devices are a 2N4416. A 150 MHz trap is included as part of the bandpass filter to preclude feed forward of the 150 MHz second LO into the IF.

The second mixer is an RCA 40821, a dual insulated gate FET. The dual gate FET is a performance choice over bipolar mixers from the standpoint of improved intermodulation products, and superior isolation of the input signal and local oscillator signals. The 40821 will provide the 11 dB conversion gain to 10.8 MHz.

The second IF is composed of a dual gate FET (RCA 40820) and a CA3089 limiter-detector integrated circuit. The CA3089 provides nominally 60 dB of log video output as well as DPSK detection by use of a quadrature detector. The min-max tolerance of log range has not been established for this device by the manufacturer.

The schematic diagram for the IF-Detector portion of the MLS receiver is shown in Figure 36. The 160.8 MHz I.F. pre-amplifier (part of the RF Head Assembly) is shown for clarity of discussion as its design is an integral part of the IF subsystem. The pre-amp and Q1 are both JFET's (2N4416) operating at 160.8 MHz and together provide a noise figure of 3 dB, a gain of 19 dB and a 3 dB bandwidth of 3.5 MHz. Rejection of the second image, occurring at 139.2 MHz in the first IF, is 60 dB. Resistor R_1 provides a 50 ohm terminating impedance for the interface coax cable from the remote RF Head.

Q2 of Figure 36 is a dual gate FET used as the second mixer utilizing the 150 MHz second LO provided by the synthesizer. The narrow band filter embodies the components from C12 through C23. This filter takes advantage of the high input impedance of the dual gate FET Q_3 to operate at a $5K\Omega$ level, ensuring high loaded Q's for the filter. The nominal 3 dB bandwidth is 250 kHz with the adjacent channel nearly 45 dB down. Other filters with steeper skirts can be provided with an increase in cost due in most part to



NOTES
1. ALL CAPACITORS ARE μF VALUES UNLESS SPECIFIED OTHERWISE
2. ALL RESISTORS ARE ¼ WATT, Ω VALUES
3. ALL INDUCTORS ARE μH VALUES

FIGURE 36. SCHEMATIC DIAGRAM, IF/DETECTOR

tune up labor. Additional IF filtering can be provided which will decrease adjacent channel response prior to limiting by another 15 dB. However, this appears to be of limited value since the IF possesses 80 dB of limiting gain.

It has been determined by AEL that the total receiver adjacent channel rejection is a more important criteria than IF adjacent channel rejection.

In other words, the primary concern is that the receiver's output to the pilot not be a response to an off channel signal. It has been demonstrated that the DPSK processing fails due to high phase distortion when the adjacent signal is operating well down on the slopes of the IF filter, effectively providing about 60 dB of adjacent channel rejection.

Log IF/DPSK Demodulator

Use of the RCA CA3089 IC was proven to be cost effective for the Low Cost MLS Receiver. Considerable testing was performed to verify the performance of this IC.

Several tests of the RCA CA3089 versus temperature were conducted to verify the RCA published performance of the level detector output (meter circuit output). The photographs shown in Figure 37 indicate the level detector output response for a typical elevation format signal; i.e., preamble and data plus "To-Fro" pulses. The meaningful data to be derived from these photographs are the consistency in pulse shapes and the variation in amplitude versus temperature. The amplitude variation, as subsequent tests disclosed, is a variation in the internal semiconductor saturation voltages (due mainly to internal bias shifts) as a function of temperature.

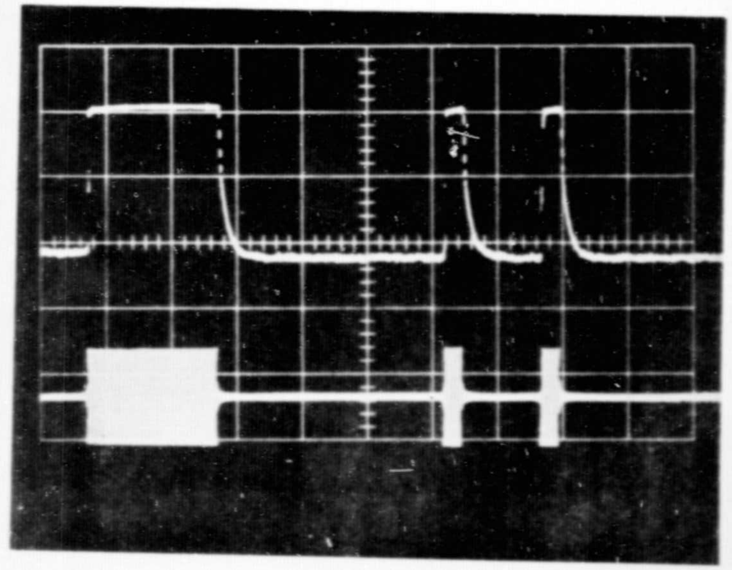
The photographs in Figure 37 show the pulse response of the CA3089 for typical MLS inputs. The pulse input level is approximately -30 dBm, the noise level is -80 dBm; hence, the output represents about 50 dB of dynamic range (roughly 20 dB/volt).

The photographs presented in Figure 38 represent a characterization of the pulse performance of the CA3089 level detector output. Of primary importance are the attack and decay times, which must not produce effective pulse stretching so as to obscure an effective pulse centroid measurement. The two photographs in Figure 38 presented are of a 100 μsecond burst and three 25 μsecond bursts. The level detector output shown represents 50 dB of range, and shows perhaps a 10 percent pulse stretch at the 50 dB down point. Some of this effect may be due to the pulse modulator used, but that is relatively insignificant. Of prime importance is the peak of the pulse and the -4 dB from peak area. This range is approximately 200 mv, and represents one of the smallest scale divisions. No significant pulse spreading is shown over this region or over at least the first 30 dB, demonstrating that the CA3089 provides an adequately large bandwidth and that no discrepancy exists between the MLS pulse measurements and CW measurements.

TOP TRACE:
LEVEL DETECTOR OUTPUT
1 V/CM

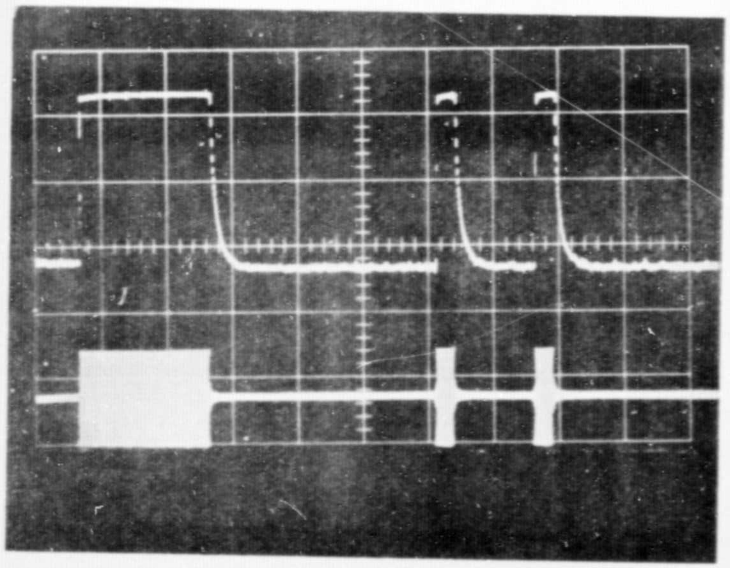
BOTTOM TRACE: 10.8 MHz
ELEVATION FORMAT

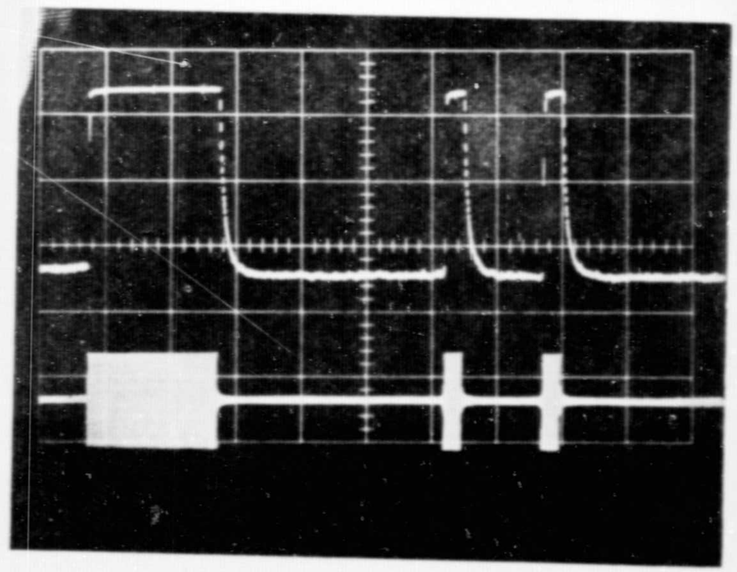
HORIZ. DISPERSION: 500μSEC/CM



A: -25°C

B: +25°C

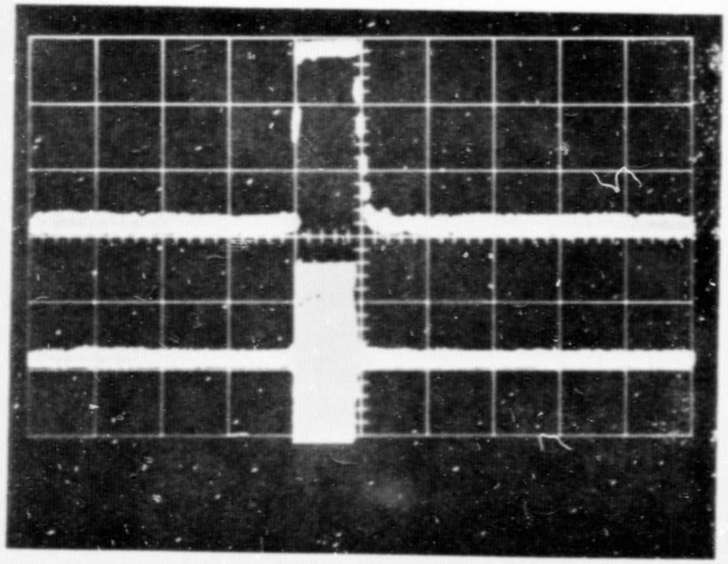




C: +75°C

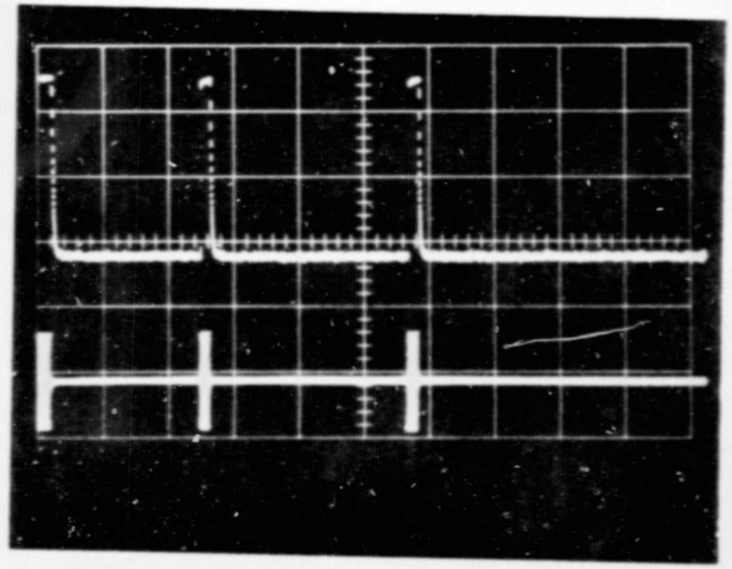
FIGURE 37. RCA CA3089 LEVEL DETECTOR OUTPUT VERSUS TEMPERATURE

TOP TRACE: LEVEL DET. OUTPUT
1.0V/DIV. - HORIZ. 100μSEC/DIV.



BOTTOM TRACE: "TO" PULSE
100μ SEC BURST.

TOP TRACE: LEVEL DET. OUTPUT
1.0V/DIV. - HORIZ. 100 μ SEC/DIV.
"TO-FRO" PULSE WIDTH 25μSEC.



BOTTOM TRACE: "TO-FRO" R.F.
BURSTS. 100μ SEC/DIV.

FIGURE 38. RCA CA3089 LEVEL DETECTOR PULSE PERFORMANCE

The performance of the log IF detector is shown in Figure 39, measured at the 160.8 MHz IF input to the receiver and thus not including the front end gain ..hich is about 5 dB. The data points are shown, with a best straight line of about 20 dB/volt.

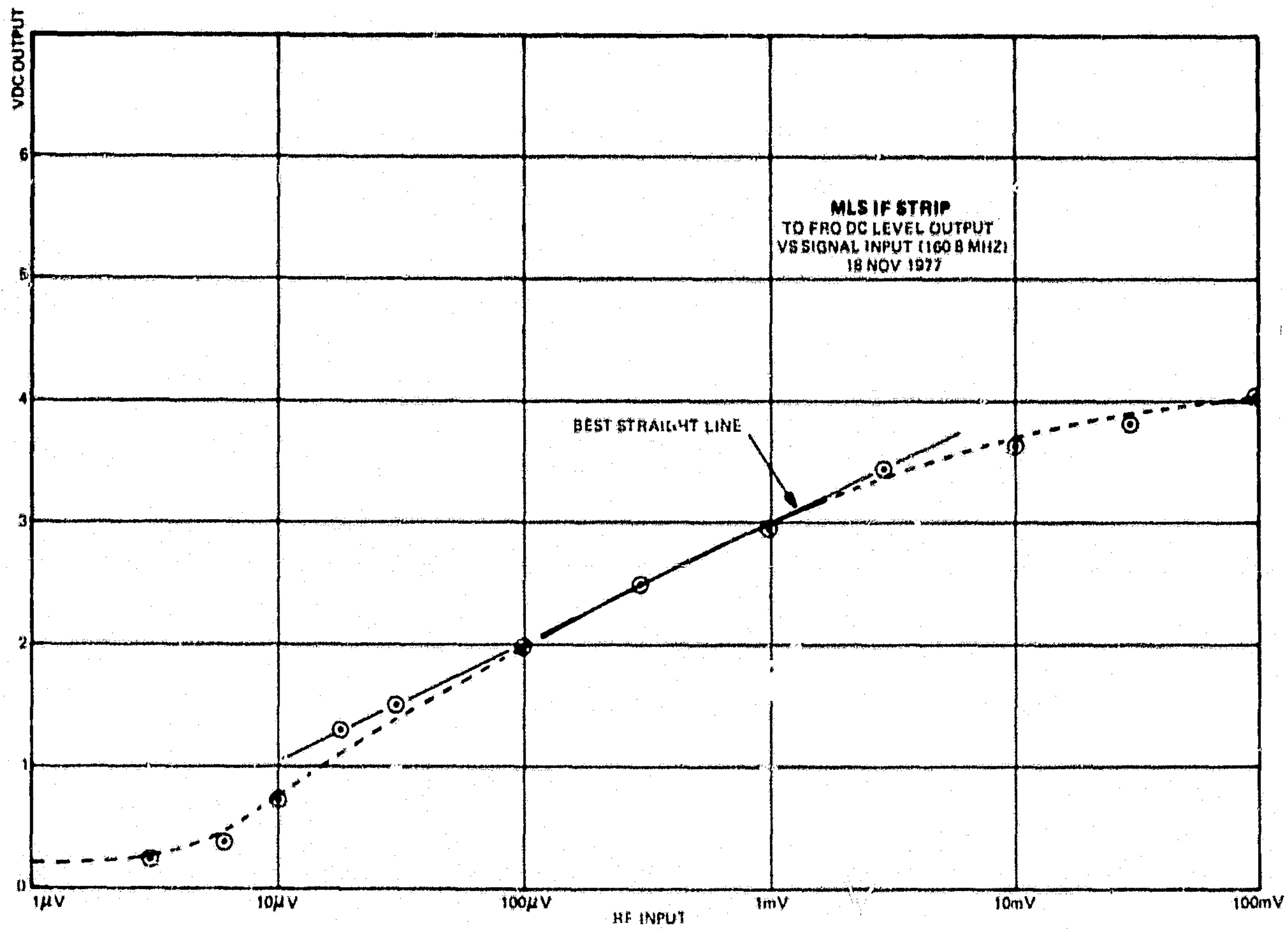
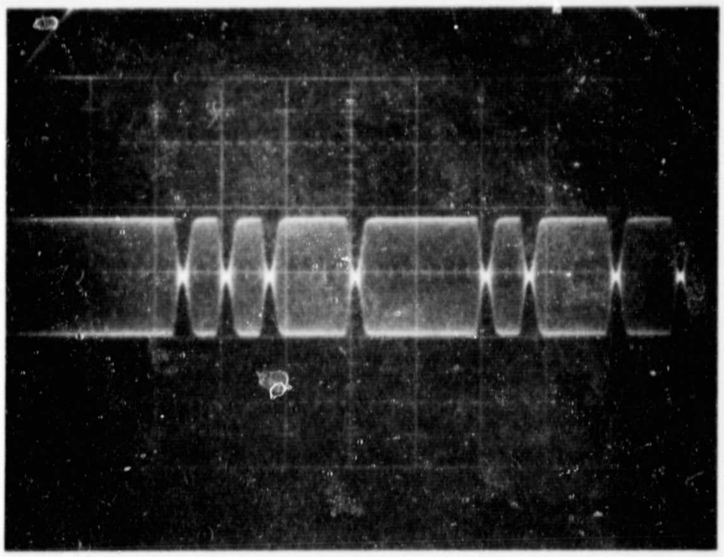


FIGURE 39. VIDEO OUTPUT VS. SIGNAL INPUT

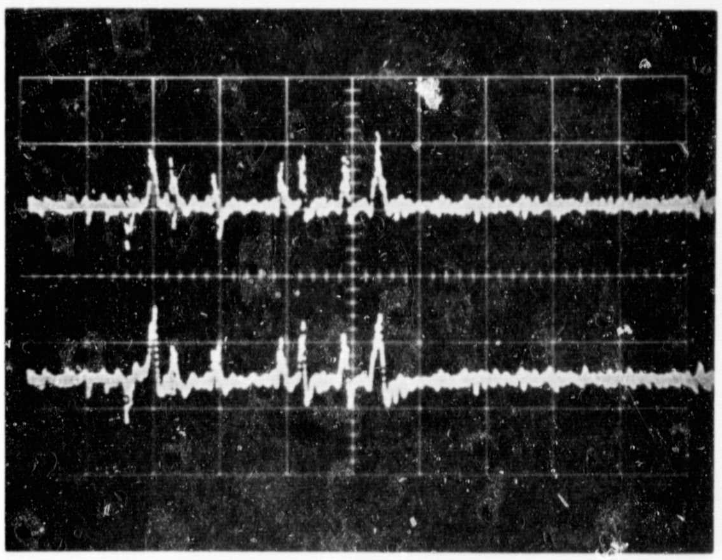
The departure from this slope is very small, less than ± 1/2 dB over the region from about 15 μ volts to about 5 mv, corresponding to -85 to -40 dBm, which is the most critical range for multipath rejection since this is the IF input voltage corresponding to where acquisition normally will occur. The specification required a ± 2 dB maximum over a 50 dB range beginning at 10 dB above tangential sensitivity.

This variation will have negligible effect on the centroid measurement, since the "To-Fro" pulses are symmetrical and the criteria for accurate measurement is that time is measured at corresponding points on the rise and fall of the pulse.



HOR. SCALE 0.1 MSEC/DIV.

FIGURE 40. DPSK TEST SIGNAL



DISC. – UPPER TRACE
PLL – LOWER TRACE
HOR. SCALE 0.2 MSEC/DIV.
9 DB INPUT S/N

FIGURE 41. DPSK DEMODULATOR OUTPUTS

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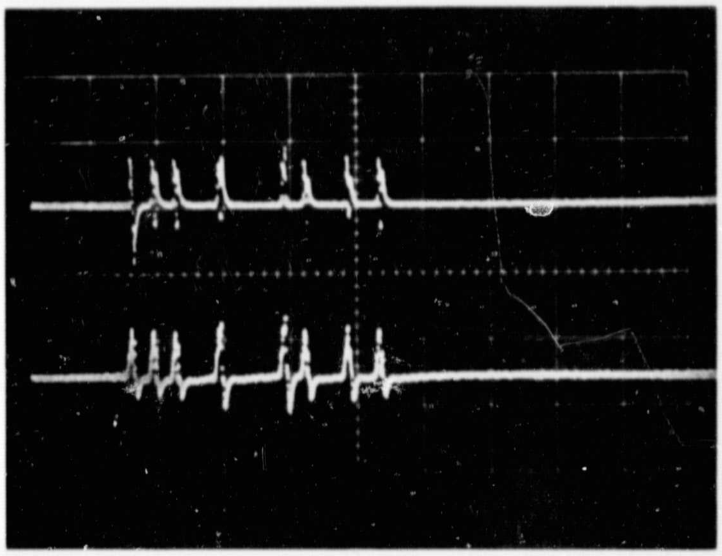
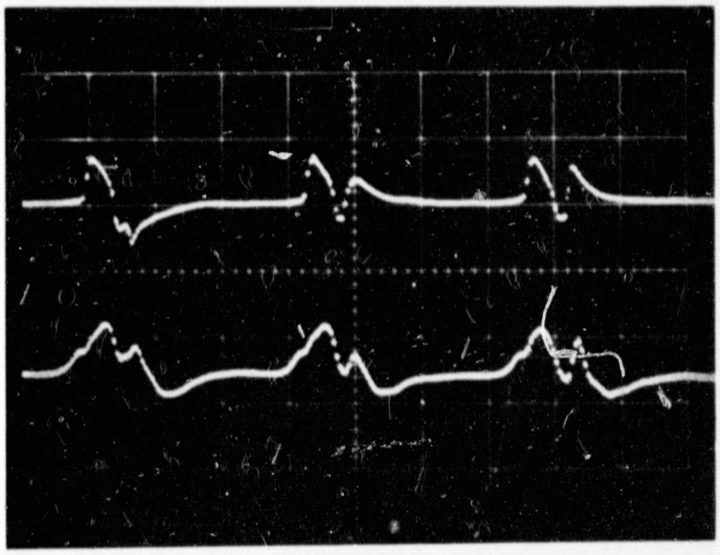


DISC. – UPPER TRACE
PLL – LOWER TRACE
HOR. SCALE 0.2 MSEC/DIV.
29 DB INPUT S/N

FIGURE 42. DPSK DEMODULATOR OUTPUTS



DISC. – UPPER TRACE
PLL – LOWER TRACE
HOR. SCALE 20 μSEC/DIV.
29 DB INPUT S/N

FIGURE 43. DPSK DEMODULATOR OUTPUTS

DPSK Detector

The detection of the DPSK data in the candidate receiver is being performed by means of a quadrature discriminator integral within the CA3089. This is an attractive technique since the circuitry required is also incorporated in the IF subsystem integrated circuit and as such requires no additional circuitry other than a few reactive components. Thus, it provides a cost advantage over alternate approaches such as a phase locked loop which would at least require a voltage controlled oscillator in addition, although it could utilize the phase detector in the CA3089. Satisfactory performance can be obtained from a discriminator as shown in Figures 40 through 43 taken early in the program prior to full receiver implementation. Figure 40 illustrates a typical MLS Barker Code and ID preamble as generated at IF by the AEL MLS signal simulator. The data pattern is 1, 1, 1, 0, 1, 0, 0, 1, 1, 0, 1, 0, 1; that is, a 5-bit Barker Code followed by a 6 bit azimuth ID, plus a trailing 0,1 which is a characteristic of the AEL test generator. The amplitude nulls occurring at the phase transitions are measured to be 44 dB in depth and are representative of the MLS waveshape. Figure 41 illustrates, simultaneously, the output of the circuit used in the MLS receiver and the output of the phase locked loop demodulator previously utilized in the AEL developed Navy MLS receiver. The large transients are the result of the phase/amplitude transitions and contain the desired information. The demodulator input signal to noise ratio is that corresponding to a -94 dBm input signal and a 15 dB receiver noise figure with a 155 kHz bandwidth (the required sensitivity of the Low Cost MLS Receiver). The video bandwidth of both demodulators is 25 kHz. The outputs may be seen to be nearly identical with the major difference being the shape of the transients. Figure 42 illustrates the same two signals with a 20 dB stronger input signal while Figure 43 shows the two signals expanded in time. In all photographs the discriminator and phase locked loop outputs can be seen to be the same.

One shortcoming of this type of DPSK demodulation is that it requires an abrupt phase switching, or "hard" switching. In later sections of this report are evaluations of actual ground transmissions using both "hard" and "soft" switching.

The DPSK demodulator function has been carefully measured, using the entire IF subassembly. The demodulator quieting sensitivity is shown in Figure 44, again not including the front end gain. The IF has 6 dB of quieting at about 4 microvolts (-95 dBm), but is just into hard limiting at that level. The addition of the front end gain of 5 dB minimum would improve this performance to about -100 dBm, if the excess noise figure contribution were not present. Actual DPSK performance, as of this writing, is in the -90 dBm range.

IF FILTERING CIRCUITS

Figure 45 shows the 160.8 MHz 1st frequency response. One of the purposes of this filter is to establish the secondary image rejection. The secondary image frequency is 21.6 MHz below the 160.8 MHz or 139.2 MHz filter center, which is also 21.6 MHz below the receiver tuned frequency. From Figure 45A, it can be seen that the response at 4.3 divisions below center is a little less than 60 dB down. This jitter also provides a rejection of about 35 dB to the residual local oscillator signal, which is 10.8 MHz below the center filter frequency. Figure 45B shows the passband in more detail, and indicates a 1.5 dB peak-to-peak passband ripple, due to the double-tuned nature of this filter.

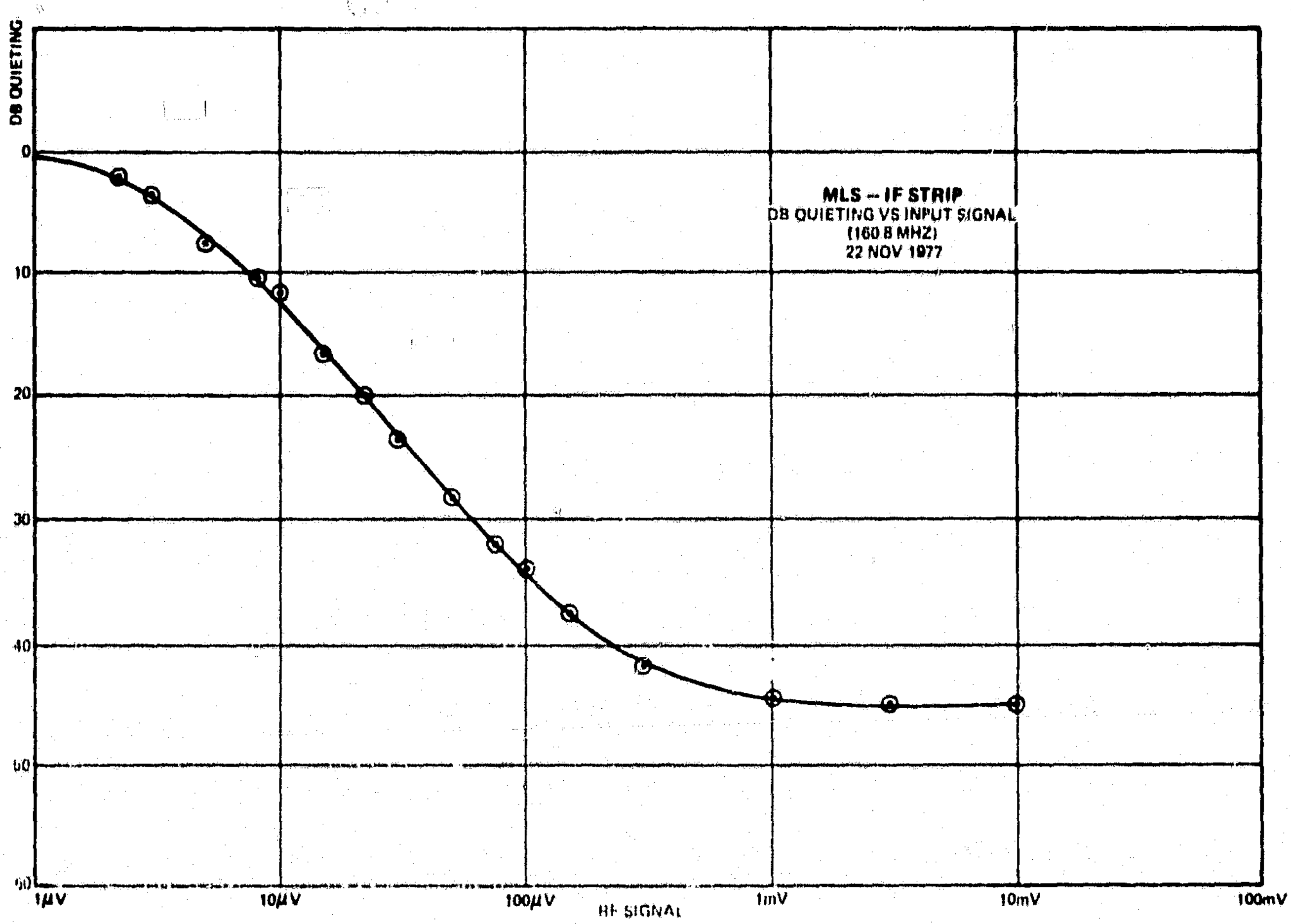


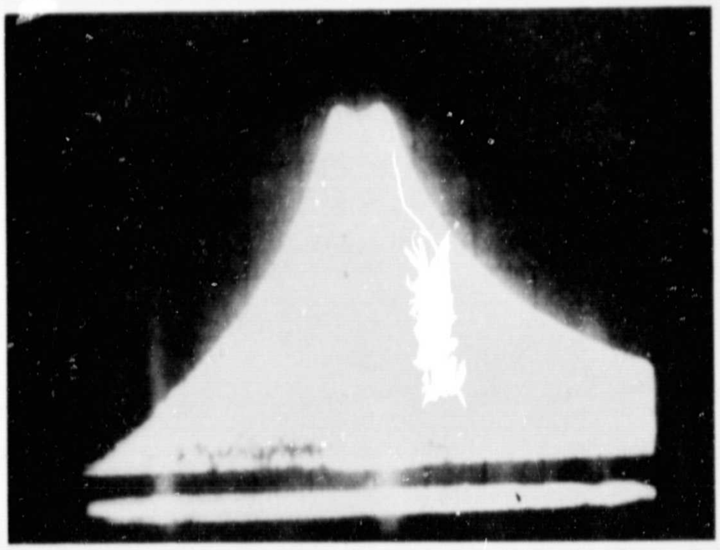
FIGURE 44. DPSK QUIETING SENSITIVITY

Second IF Stage

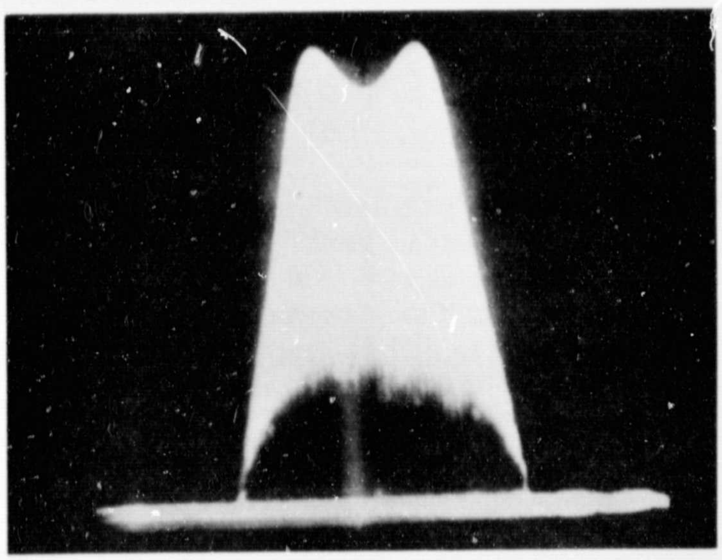
Considerable attention has been placed on the 2nd IF filtered stage, due to the significant impact on material cost as a function of filter parameters. It was determined that an LC filter would be more cost effective than a crystal type, and could be accomplished with a three-resonator LC type. The circuit for this filter is composed of C_{12}, C_{14}, C_{15}, C_{16}, C_{19}, C_{21}, C_{22} and C_{23} with L_6, L_8 and L_9, all of which were shown in Figure 36. This filter has been designed for easy alignment and low material cost.

Figure 46A shows the 10.8 MHz 2nd IF frequency response at 10 dB/division. The 3 dB bandwidth of this stage is about 225 kHz. The response to a signal in an adjacent channel is -45 dB at -295 kHz and -47 dB at +295 kHz.

Figure 46B shows the stage response at 2 dB/division. The ripple is less than 0.5 dB peak-to-peak.

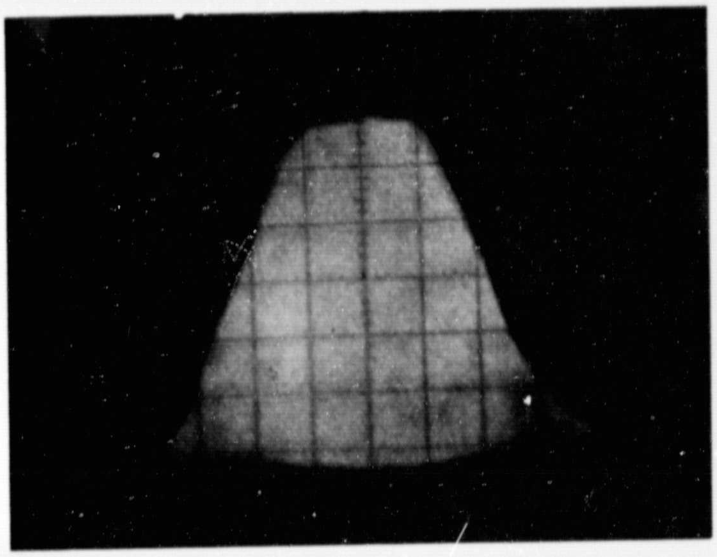


A) Swept Frequency Response
10 db/div. vertical,
5 MHz/div. horizontal,
160. 8 MHz center

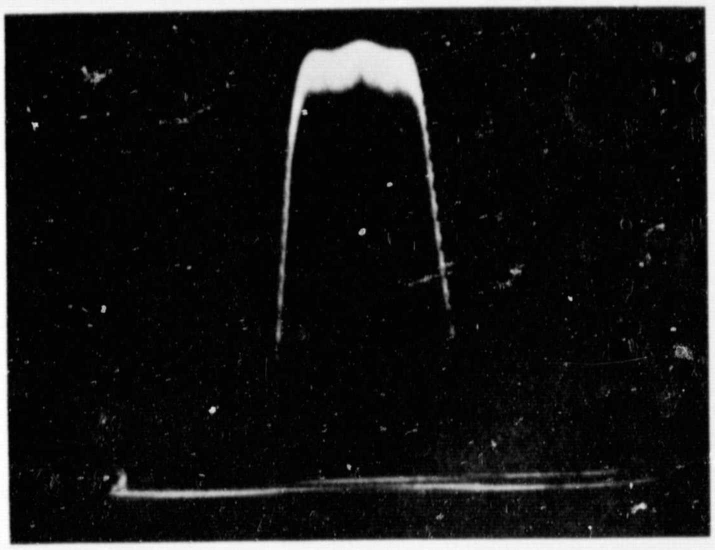


B) Swept Frequency Response
2 db/div. vertical,
2 MHz/div. horizontal,
160. 8 MHz center

FIGURE 45. RESPONSE OF 160.8 MHz IF



A) Swept Frequency Response
10 db/div. vertical,
0.1 MHz/div. horizontal,
10.8 MHz center



B) Swept Frequency Response,
2 db/div. vertical,
0.1 MHz/div. horizontal,
10.8 MHz center

FIGURE 46. RESPONSE OF 10.8 MHz IF

IF/DETECTOR CONSTRUCTION

The top view of the IF/Detector assembly is shown in Figure 47, complete with shielding in place. Figures 48 and 49 show the top and bottom views respectively. Figure 50 is an assembly drawing of the IF/Detector board.

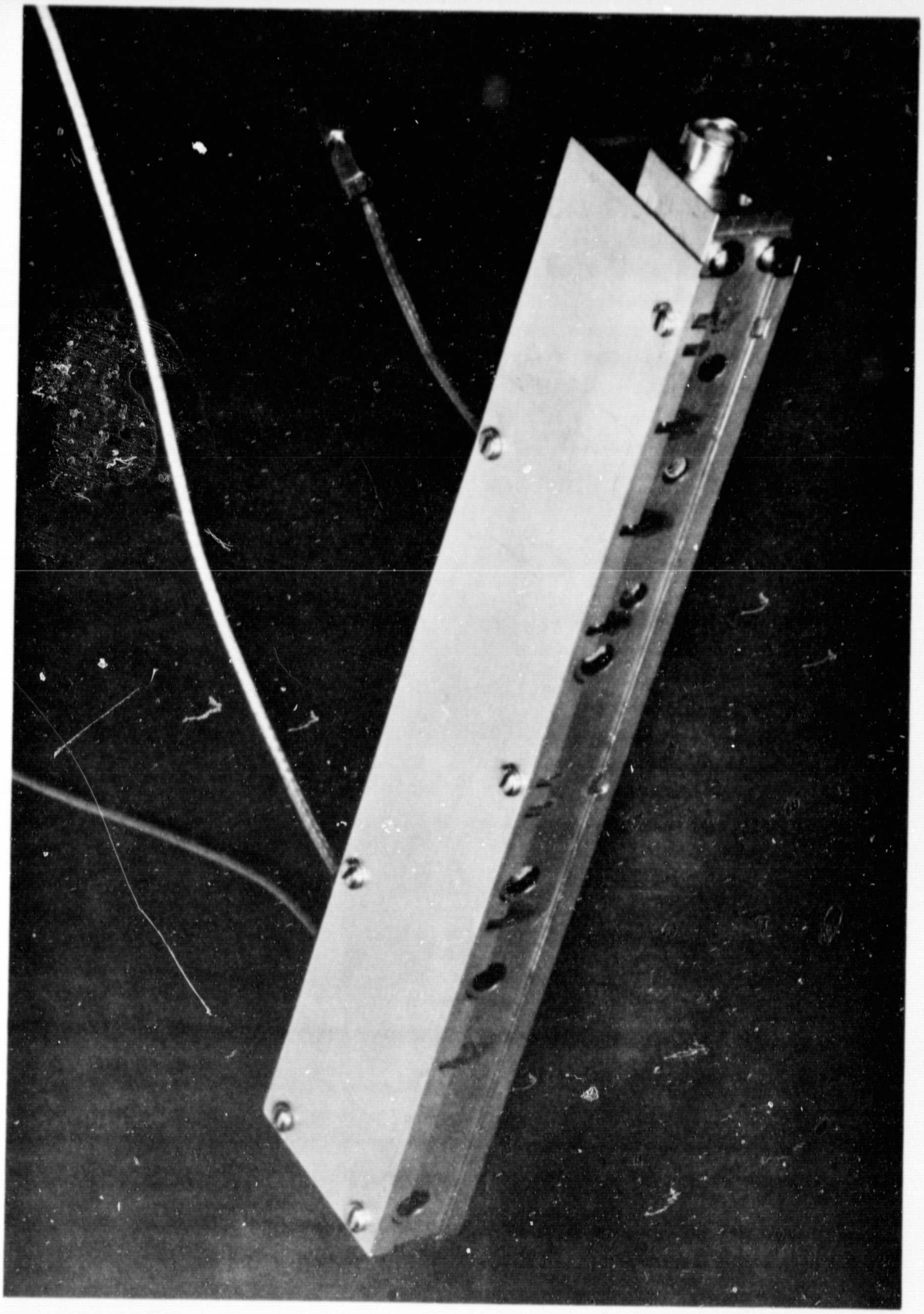


FIGURE 47. IF/DETECTOR ASSEMBLY TOP VIEW

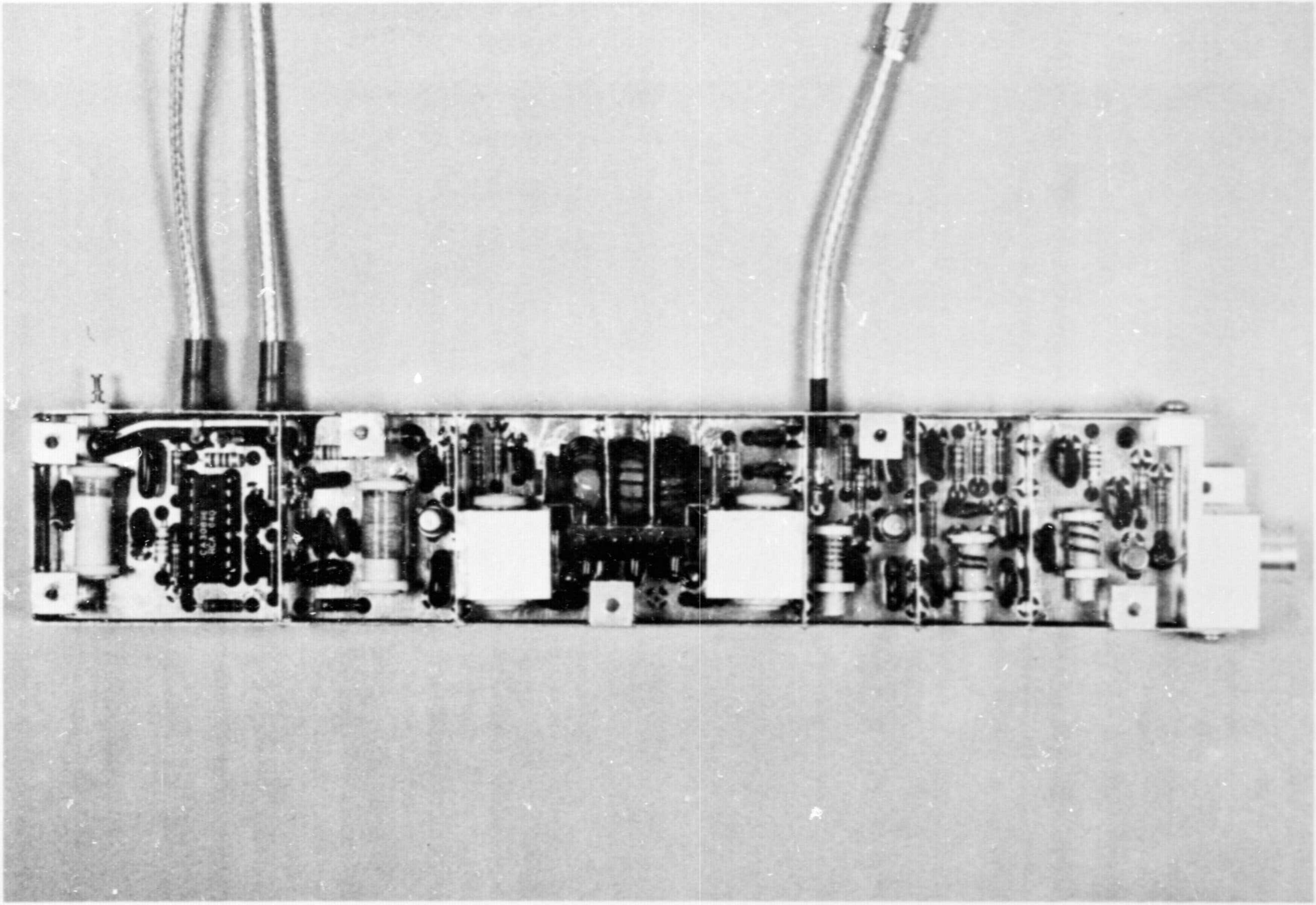


FIGURE 48. IF/DETECTOR TOP SIDE

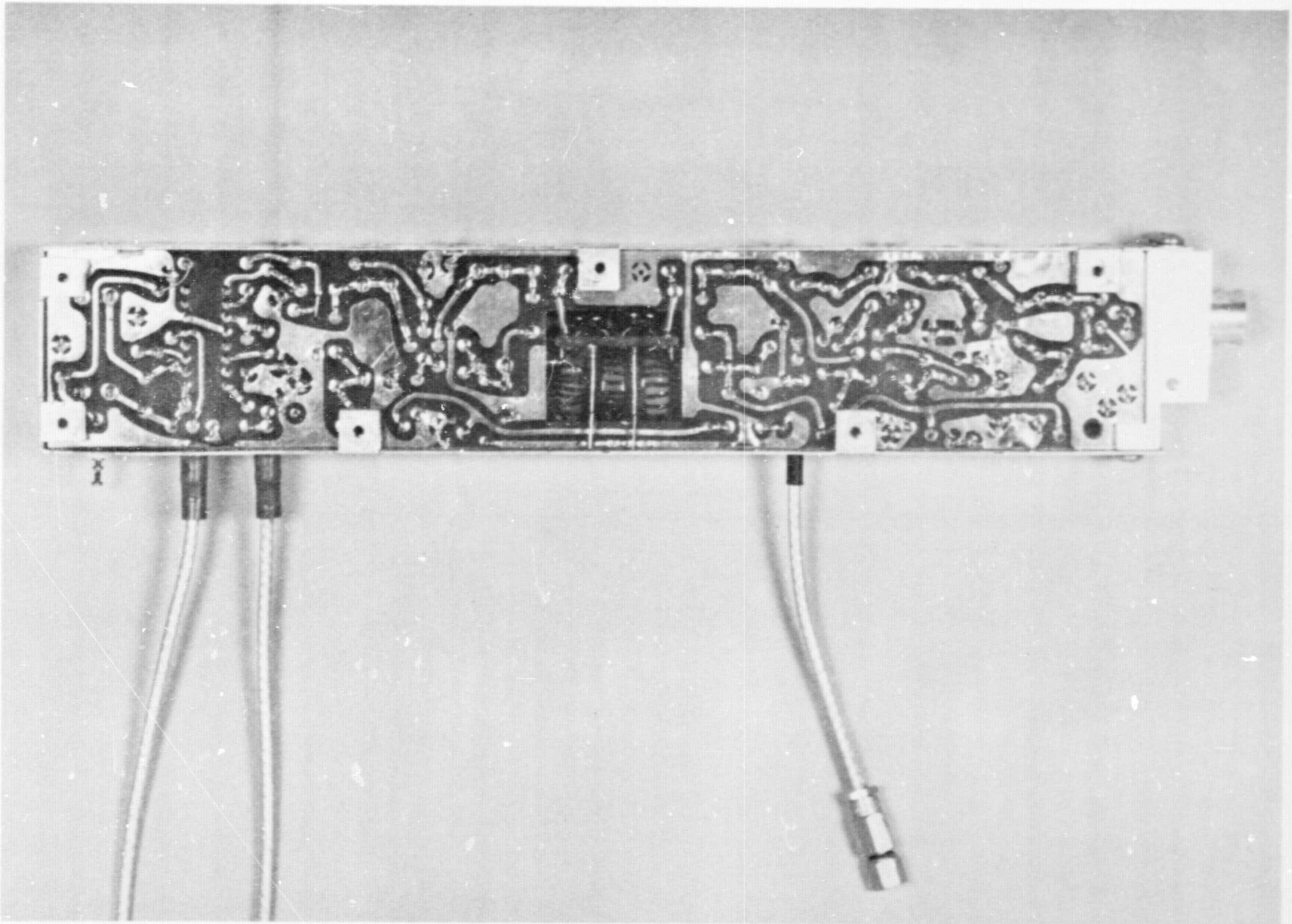


FIGURE 49. IF/DETECTOR BOTTOM SIDE

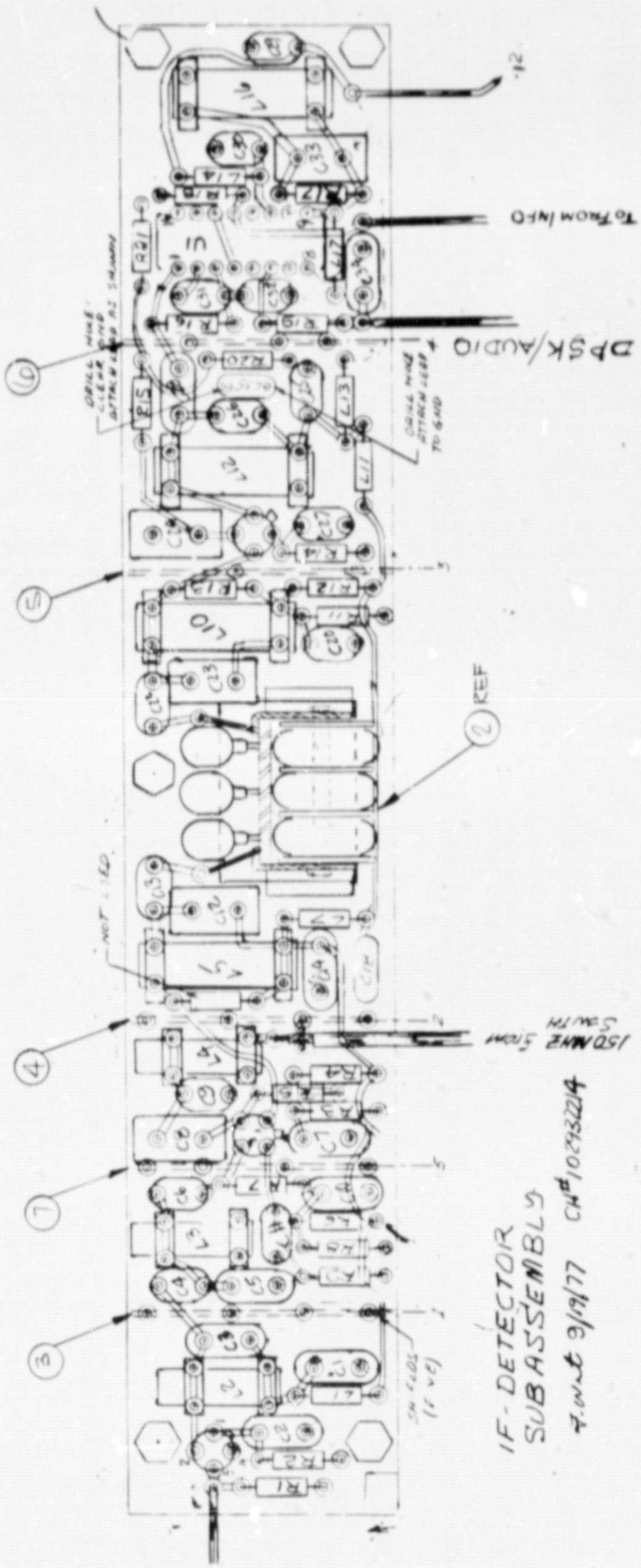


FIGURE 50. BOARD ASSEMBLY, IF/DETECTOR

PROCESSOR ASSEMBLY

The Processor Assembly operates on the detected log video and DPSK output of the IF/Detector Assembly such as to produce course deviation and flag outputs to the CDI display. The Processor Assembly is composed of two circuit areas: the first is an analog preprocessor circuit and the second is a microprocessor oriented digital processing circuit.

Analog Preprocessor

The major functions of the analog preprocessor are to:

- Provide strobe pulses to the real time processor which define the leading and trailing edge of each to-fro pulse
- Discriminate against low to moderate level pulse interference
- Provide sidelobe suppression
- Interface the DPSK demodulator with the mocroprocessor including clock recovery.

The first three of these functions are performed by a peak detector/charge coupled device (CCD) delay line/comparator circuit which holds the peak level of a received pulse and then compares the level of delayed (via the CCD) version of this pulse with a voltage equal to 4 dB below the peak pulse level. Thus, the output of the comparator consists of pulses equal to the 4 dB width of the received scanning beam. A bidirectional one-shot generates 1μsec pulses on the leading and trailing edge of each pulse from the comparator. The generated pulses occur at some time after (the delay through the CCD) the actual received pulses but, since both the "to" and "fro" pulses are subject to the same delay, their separation is preserved. Signals more than 4 dB below the largest signal and occurring after it will provide no output since they will fail to exceed the threshold. Likewise, in the sidelobe region, the SLS pulse will establish a threshold which the sidelobes will fail to exceed. The peak detector is reset prior to the SLS pulses of each function and again at midscan so that a new threshold is set for both "to" and "fro" pulses, thus allowing operation under conditions of propeller modulation where the pulses may differ in amplitude by 6 dB. Use of this peak detector/delay/threshold technique thus economically provides the receiver with adaptive capabilities on a scan by scan basis, enhancing its ability to operate under adverse conditions. While the required time delay could be provided by an LC delay unit, the size of such a network would be prohibitive; thus, the use of the CCD analog delay which, even considering the required clock circuitry, requires a minor amount of space. The remaining analog preprocessor function is that of recovering the data and data clock from the DPSK signal format. Figure 51 shows the block diagram for this signal processing. A dual one-shot (74L123N) and clocked oscillator (NE555) provide the simple, inexpensive, and reliable data decoder.

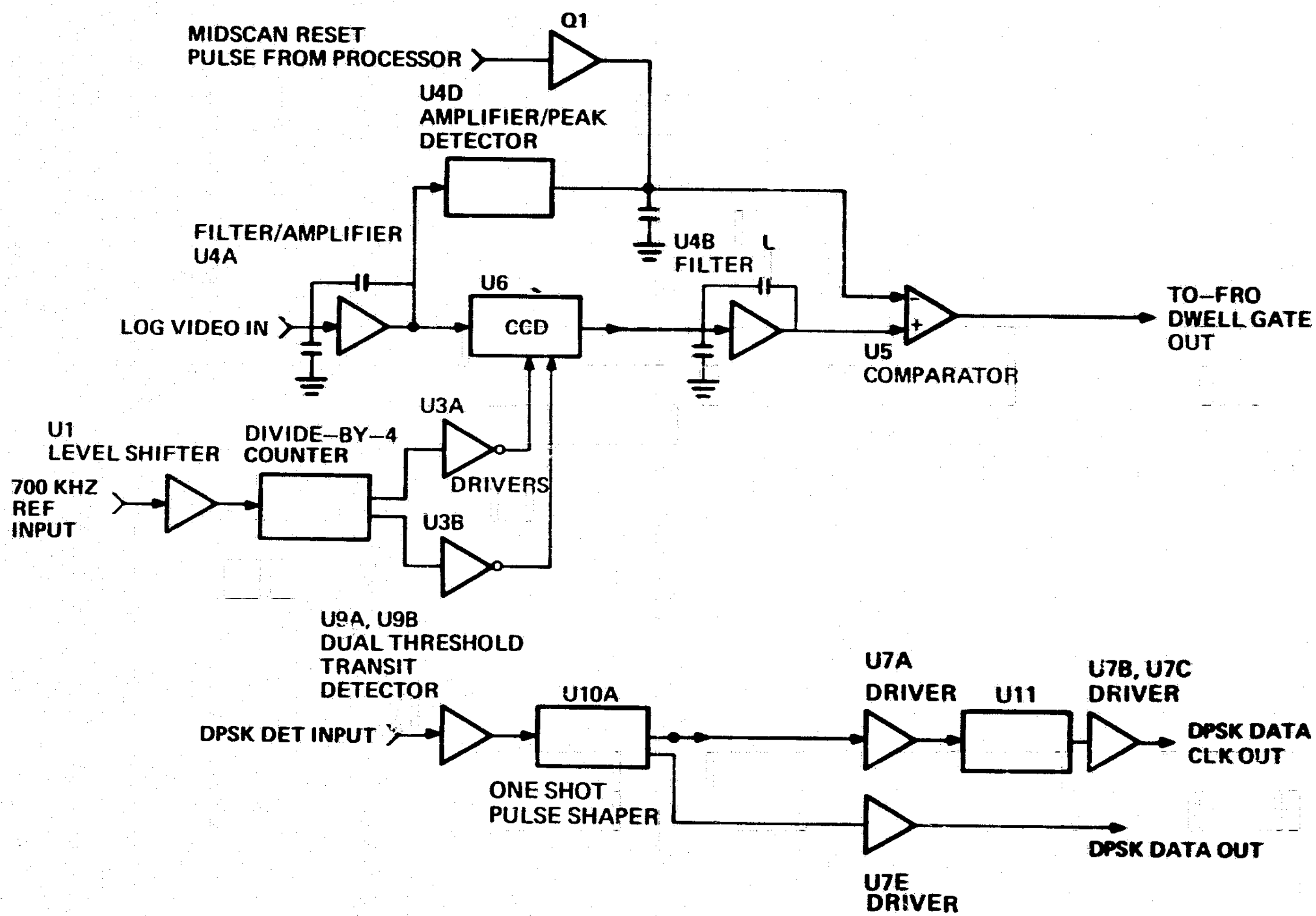


FIGURE 51. PREPROCESSOR BLOCK DIAGRAM

Dwell gate generator. - The circuit for the Dwell gate generator is included in the Preprocessor schematic of Figure 52.

The log video input is filtered by U4A and applied to both the delay line U6 and as a DPSK squelch enable to U10A.

The CCD device provides a 231 microsec delay to the To-Fro video signal and U4A, B, and C provide the necessary filtering and pulse shaping. The low pass response of this circuit is 3 dB down at 30 KHz. The non-delayed pulse is amplified by U4D and drives the peak detector CR1 and C3. The LM 211 (U5) makes the final level comparison and provides To-Fro dwell gates equal in width to the To-Fro 4 dB pulse width. Q1 provides resetting of the peak detector at mid-scan and prior to the "to" scan.

The clock timing for CCD delay line U6 is supplied by the dual drivers U3A and U3B, both being gated at 400 kHz rate by divider U2. Since the delay line U6 is a 185 section CCD type, 185 cycles at 400 kHz produces a 231 microsecond delay. The input to divider U2 is the 1.6 MHz clock from the synthesizer assembly.

DPSK demodulator. - The circuit for DPSK data and clock recovery is also shown in Figure 52. The bi-directional comparators U9A and U9B provides a clean, constant level data format to U10A which is a 15 μsec one shot. Integrated circuit U7A triggers and synchronizes the free running NE555 clock. The data clock is further shaped by one shot multivibrator U10B and applied to U7B, U7C for output drive. The recovered data is derived from the Q output of U10A and the 15 kHz data clock from the NE555.

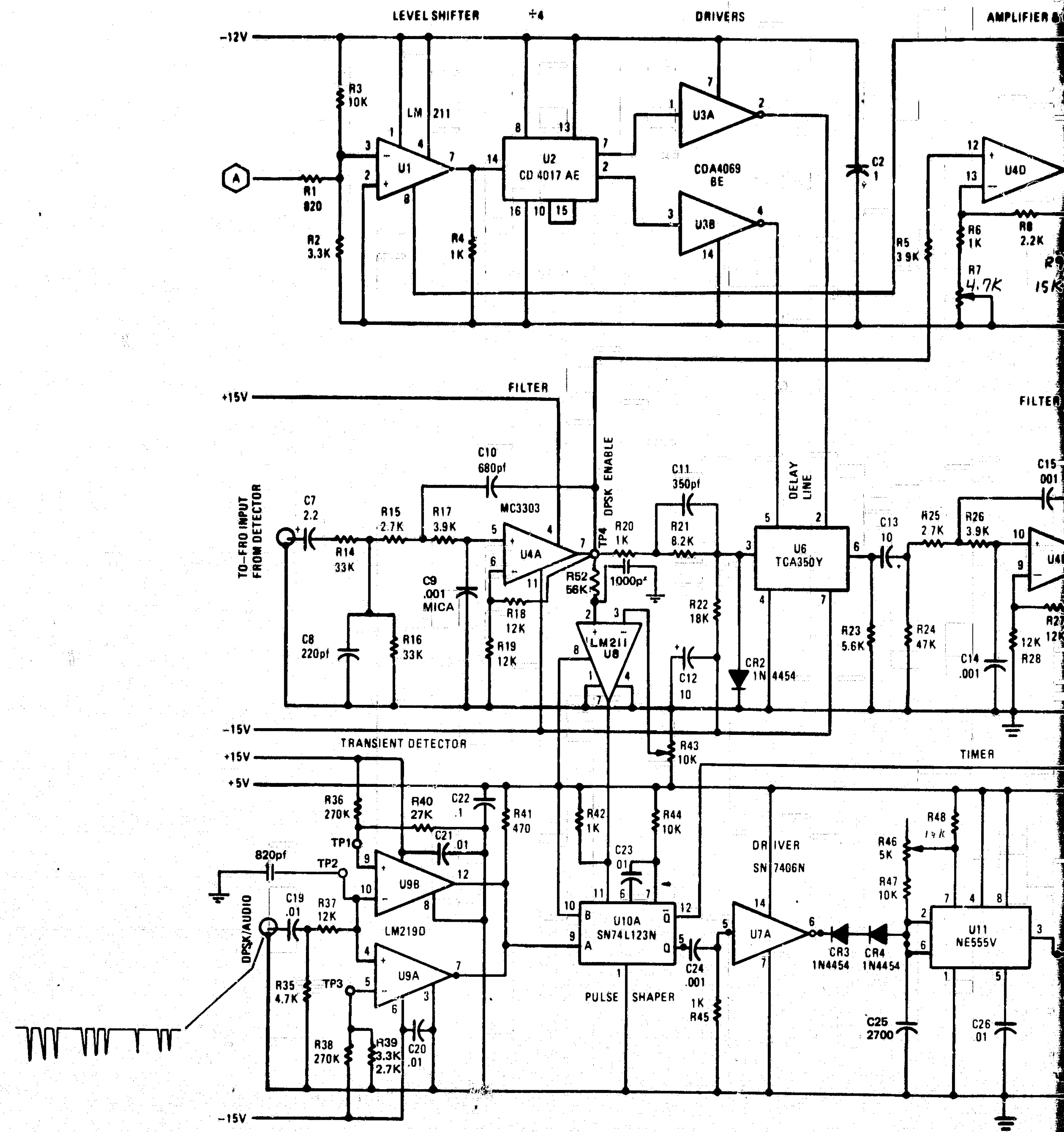
Microprocessor Selection

In selecting a microprocessor for general aviation usage, the important factor is overall processor system cost, which was the principal reason for selecting the MOSTEK 3850 as the primary choice for the low cost MLS system.

Although there are other microprocessors in the same price range with the 3850, the major superior virtue is its I/O structure. Since the address bus has been omitted from the 3850 architecture, 16 lines on both the CPU chip and the ROM chip have been freed to be utilized as I/O lines in the directly addressable I/O structure. This allows the user to service 4 independent 8-bit I/O parts from software and remove the cost of the data bus in the system price.

In any system, the 3850 becomes a leading candidate for the entire spectrum of general aviation equipment, since most general aviation systems must service more than one I/O; i.e., switches, synthesizers, and other I/O's.

A Low Cost MLS microprocessor tradeoff chart is shown in Figure 53. The 3850 microprocessor is an excellent candidate in all respects.



FOLDOUT FRAME 1

C-2

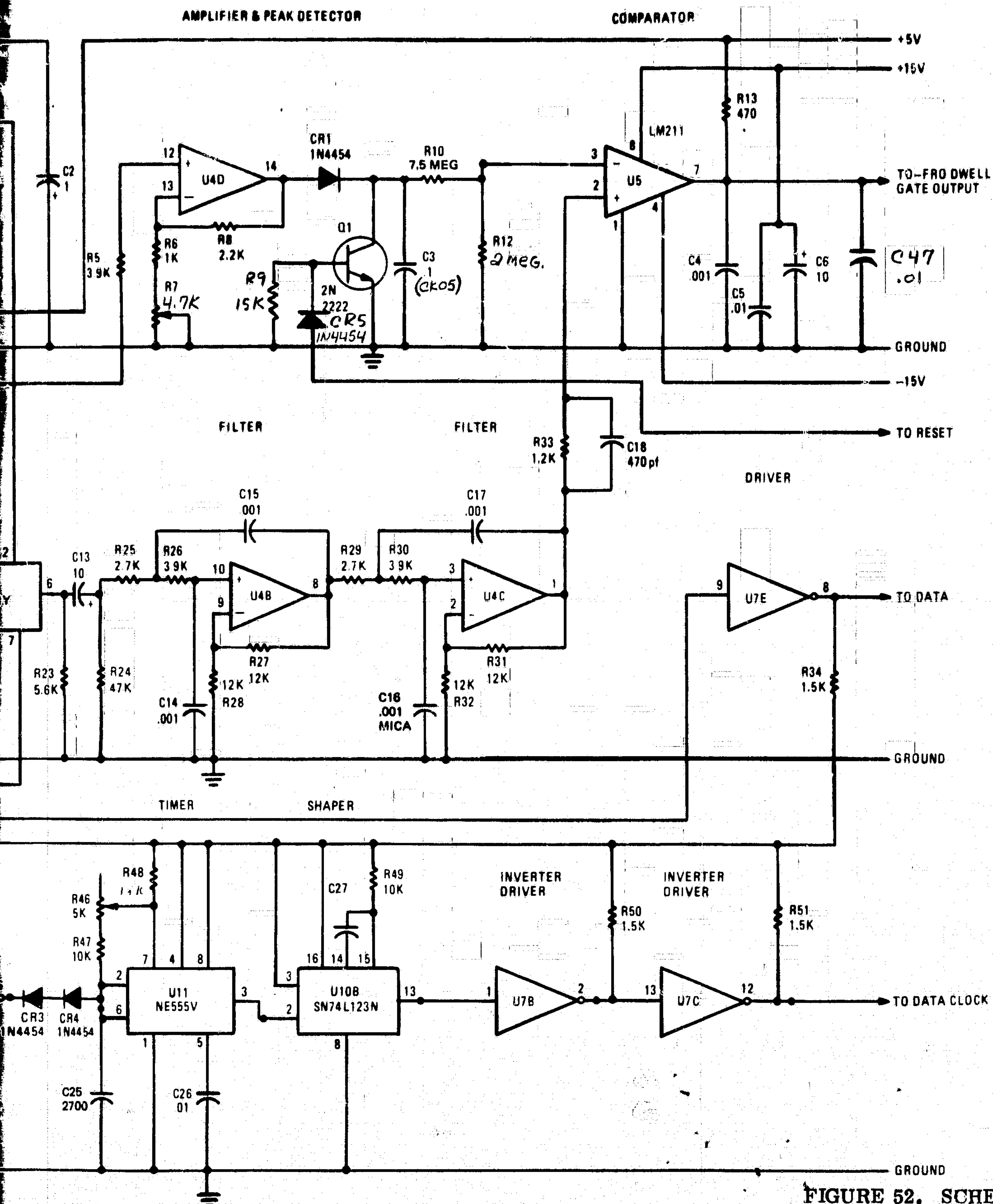


FIGURE 52. SCHEMATIC DIAGRAM PREPROCESSOR

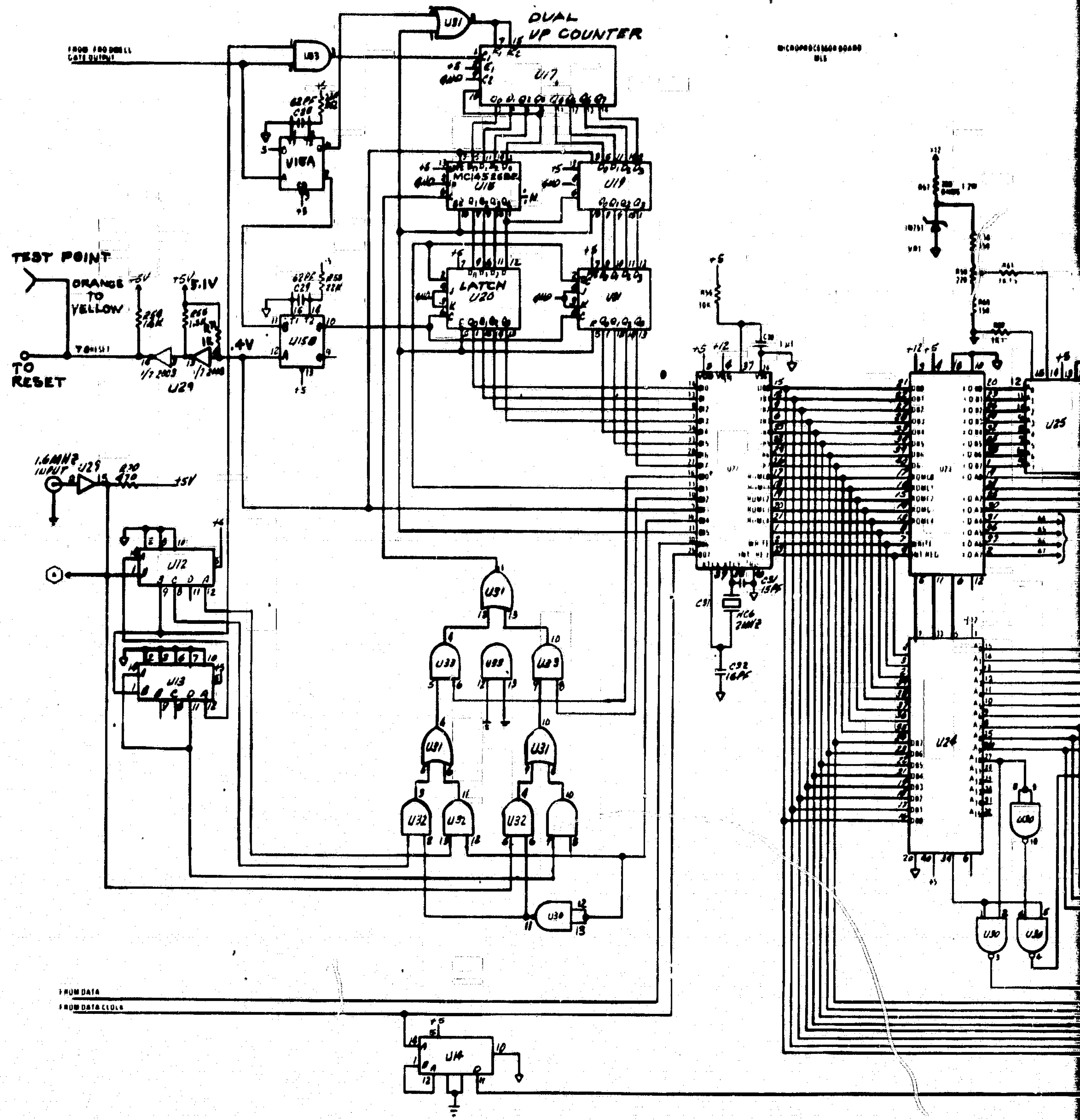
FOLDOUT FRAME 2

	MINIMUM PKG/PROC.	SECOND SOURCE	MIN. ORDER	EXTERNAL SUPPORT LOGIC	SYSTEM EXPANSION	SYSTEM COST	NO. OF INSTRUCTIONS IN SET	CYCLE TIME μSEC
TSM 1000	1	NO	5K	LARGE	VERY POOR	MED.	43	12.0
SC/MP	3	YES?	1	MEDIUM	EASY	MED.	46	2.0
6800	5	NO	1	LARGE	EASY	HI	72	1.0
8080	5	YES	1	LARGE	EASY	HI	78	2.0
3850	2	YES	100	LOW	EASY LOST-PARTS	LOW	76/101	2.0
CDP-1802	3	NO	1	MEDIUM	MEDIUM	MED.	91	2.5
IM6100	3	YES	1	MEDIUM	MED.	MED.	40+	1.5

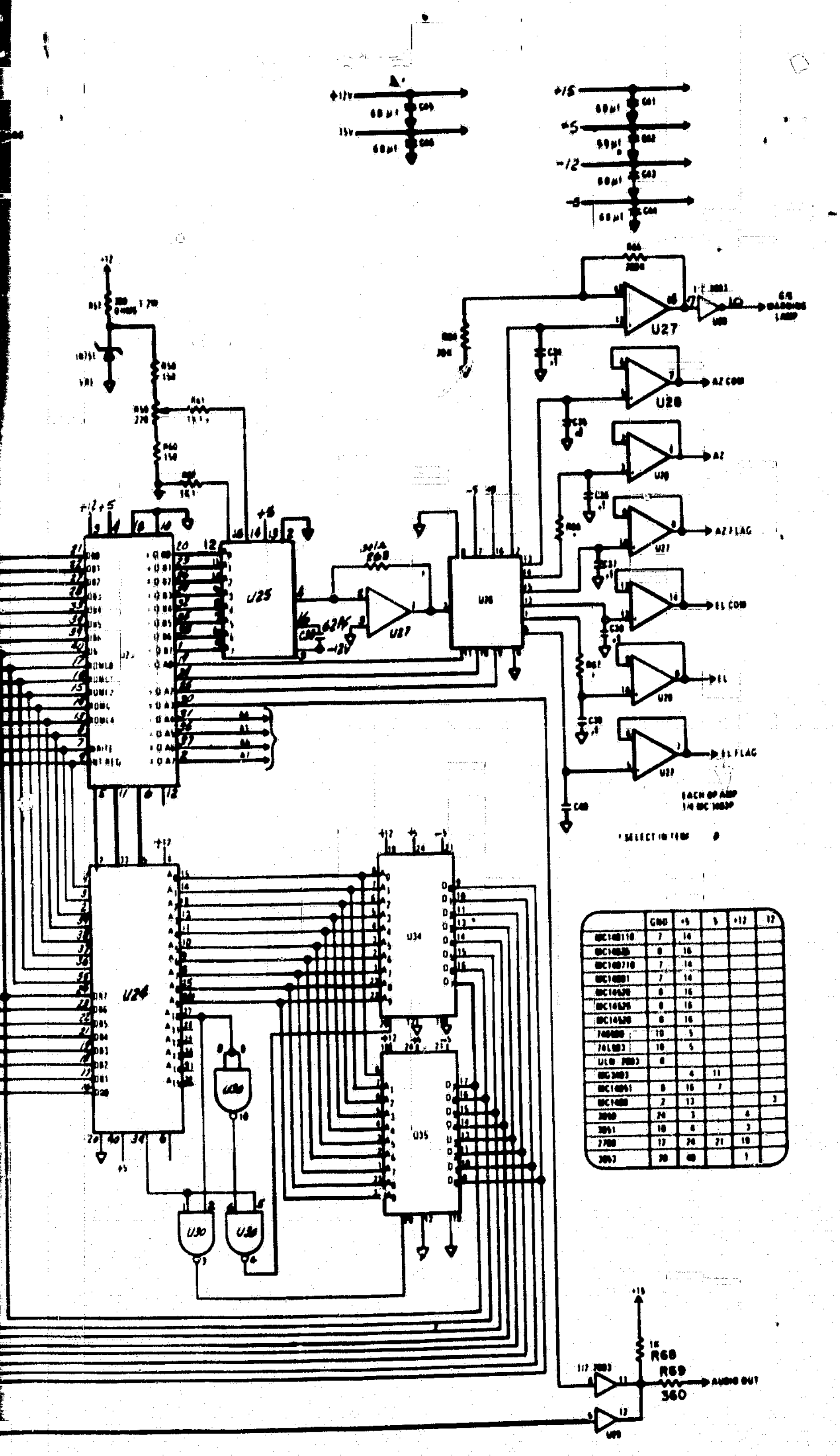
FIGURE 53. MICROPROCESSOR TRADE-OFFS FOR THE MLS RECEIVER

Processor Circuitry

The MLS processor schematic is shown in Figure 54. Integrated circuits U12, U13, U30, U31, U32 and U33 provide timing countdown and control from the 1.6 MHz master clock.



FOLDOUT FRAME



	GND	+5	-5	+12	-12
[illegible]	7	14			
[illegible]	8	16			
[illegible]	7	14			
[illegible]	7	14			
[illegible]	8	16			
[illegible]	8	16			
[illegible]	8	16			
[illegible]	10	5			
[illegible]	10	5			
ULN 2003	8				
[illegible]		4	11		
[illegible]	8	16	7		
[illegible]	7	13			3
[illegible]	24	3		4	
[illegible]	10	8		3	
[illegible]	17	24	21	19	
[illegible]	20	40		1	

FIGURE 54. SCHEMATIC DIAGRAM, PROCESSOR

FOLDOUT FRAME 2

DETAILED PROCESSOR OPERATION

The digital processor assembly can be divided into two functional areas: the Real Time A/D Converter, and the output.

Real Time A/D Converter

The A/D converter consists of counters U17, 18, 19, 20 and 21, supporting Single Shot (SS) U15A, B and clock selection gates U31, 32, and 33.

The principle used in the A/D is that the angle to be determined is divided up into 256 equal parts. This is done by gating a clock to the counter chain U18 and U19, the frequency which will determine the basic resolution of the function/mode. Therefore, the lowest frequency clock (40 kHz) would be in Az search mode when 132° of arc are being searched, and the highest frequency clock (1.6 MHz) is in the EL track mode when full scale meter deflection is only 0.7°.

As an example of the A/D operation assume that the microprocessor has called for the function "Azimuth" by a "high" on its ϕ00 output and the search mode by a high on its ϕ04 output. This will allow clocks from U31 pin 11 to toggle counters U18 and U19. When a video data signal is received on the dwell gate line, it will enable "AND" gate U33 to clock the pulse width counter U17, and at the same time the dwell pulse leading edge will fire the single shot U15A. The width of the pulse generated by U15A is narrow (less than 1 microsec). This pulse resets the pulse width counter U17 and fires the other half of the dual one shot U15B. U15B is used as an "OR" gate as well as a one shot in that it is also fired at its "A" input by the microprocessor. The output of U15B is used to clock the output state of the counters U18 and U19 into the data latches U20, and U21.

At the end of the "TO" scan the position of the received dwell pulse with respect to the generated search gate is stored in the latches U20, U21. At this time the microprocessor will read its parallel input ports ϕ10 thru ϕ17. After reading that data (dwell location) it will generate a strobe pulse on port ϕ03 which will strobe the contents of the pulse width counter U17 into the parallel inputs of counter U18 and U19.

Next the microprocessor will generate another strobe on port ϕ03 that will transfer the data from U18, U19 into the data latches U20. U21 and the microprocessor will read the latched data. The processor now has the location of the leading edge and pulse width of the dwell pulse (the last one only) received during the search gate in the Az function. At the end of the mid scan time period the processor would again generate the same gates and read the data in the same manner with the exception that when the position data was read, the true/complement line of the data latches, pin 2, would be put in the complement mode before that data was read. The reason for this is as follows: if on the "TO" scan the dwell pulse were ten clocks below the 0° position (HEX7F) the

counter would read HEX 75, on the "FRO" scan the dwell pulse would be 10 clocks above the 0° position or HEX 8A (binary 1000 1010) and if this number is complemented we have HEX 75. This simple routine in reading the data removes the need for complementing and the "FRO", or "UP" data inside the processor.

Output

The output section is made up of an 8 bit D/A converter and a 1 line to 8 line multiplexer with seven operational amps to form a 7 line sample and hold. These are used to drive the meter/autopilot outputs. The D/A converter chip, U25, uses the microprocessor output ports I/O Bϕ through B7 as inputs. This is a commercial D/A chip whose current output at pin 4 is converted to a voltage source by operational amp U27. The output of U27 is then steered to the appropriate sample and hold (S/H) by the multiplexer U26. The multiplexer is addressed by the I/O ports Aϕ, A1, A2 of the microprocessor in the following code.

Aϕ	A1	A2	Aϕ	A1	A2
0	0	0 AZ Com	0	0	1 EL
1	0	0 AZ	1	0	1 EL Flag
0	1	0 AZ Flag	0	1	1 G/S Warning Lamp
1	1	0 EL Com.	1	1	1 Not used

The ident bit which controls the station identification tone is I/O A3.

All outputs conform to the low level requirement of DO-132.

Processor Software

During the development, particular effort was expended on optimizing the Data Word identification subroutines and the confidence subroutines. A software flow chart is shown in Figure 55, followed by the complete software listing. The octal designations placed at the upper left hand corner of each software action block refers to the listing number. Comments to the MOSTEK 3850 assembly language are shown on the right of the listing.

A more detailed description of the microprocessor routines is as follows:

Initialization	This part of the program clears all averaging registers, ensures that the flags are displayed, and clears confidence counters.
Read DPSK Data Barker Code?	Here, both the DPSK data and clocks are read, the data is shifted right in an internal register and compared with the known bit pattern for the Barker code until it is recognized. After the Barker code is recognized, the DPSK bit pattern is compared with the four stored function identifications (azimuth,

elevation, data word 1 and 2). If a function identification is recognized and parity is correct, the appropriate action is taken by the microprocessor. If the identification is not recognized, the processor goes back to its task of servicing the outputs and reading DPSK.

Identify Function

Here, if the ID and parity are recognized, the proper action will be taken by the microprocessor; this includes: 1. Basic Data Word 1, bits I20 and I21 = 00 Flag Azimuth Function: 2. Basic Data Word 2, bits I_{27} and I_{28} = 00 Flag Elevation Function: 3. Elevation and Azimuth Functions are similar but only Azimuth is discussed in this example.

Azimuth
Read Morse Code
Check if Search or Track

If the Azimuth ID is recognized, the processor continues to count DPSK clocks and data and uses bit I_{12} for Facility Identification, and on Clock 37 enables the Azimuth gate to allow the azimuth clocking. The Morse code is then read and the Morse code set to its proper state. The azimuth clocking has two modes: Search (wide scan) and Track (narrow scan). In the Search Mode the entire scan is covered by the 8-bit counter or 132°/256 bit or $\approx 0.5°$ bit. In Search Mode, if it is found that the To-Fro pulses are in the center 1/3 locations the processor will go into the Track Mode. In the Track Mode the gate is enabled only in the center 1/3 of the scanning period and the clock enable is 5 times the frequency of the search clock or now 44/256 or $\approx 0.17°$/Bit accuracy.

The sequency of events in the program are as follows:

Begin TO scan. Enable gate if in Search Mode.

Enable gate if in Track Mode.

Inhibit Track gate.

End TO scan, inhibit Search gate.
1) read data latch
2) strobe pulse width center in data, etc.
3) strobe data center (pulse width) into data latch
4) read pulse width
5) reset counters and CCD memory

Start FRO scan enable gate if in Search Mode.

Enable gate in Track Mode.

Inhibit gate in Track Mode.

Inhibit gate in Search Mode end FRO scan
1) read data latch
2) strobe pulse width center into data center
3) strobe pulse width into data latch
4) read pulse width
5) reset counters and CCD memory

Pulse Width Test	TO and FRO. If the pulse width passes the test, (not too wide or narrow) the next test is performed. If the pulse width test failed, the confidence center is decremented and the processor searches for a new Barker code.
Colocation Test	The position of the TO pulse is checked against the position of the FRO pulse to ensure colocation. If yes, the next sequence is performed. If no, the program returns on the same line as a failure of pulse width.
Confidence Subroutine	If the preceeding test has been passed, the confidence center is incremented and if enough confidence has been established the flag is lifted.
Average Routine	The average and output portion of the program performs a running average of 8 data and 8 pulse width readings. The averaging increases the basic resolution of the data by a factor of 8, therefore, the azimuth data resolution is $0.17°/8 = 0.02°$. The data is outputed to an 8 bit D/A which has 2 times full scale drive output, since full scale is $\pm 2.5°$. 2X is 10° total and $10°/200 = 0.05°$/bit.

PROCESSOR CONSTRUCTION

Figures 56 and 57 respectively show the top and bottom views of the processor assembly. Figure 58 shows the assembly drawing.

In figure 56, the analog components are associated with the preprocessor and occupy the bottom and lower left portion. The large packaged microprocessor and memory portions of the processor occupy the right hand side.

The processor utilizes 1024 bytes of memory.

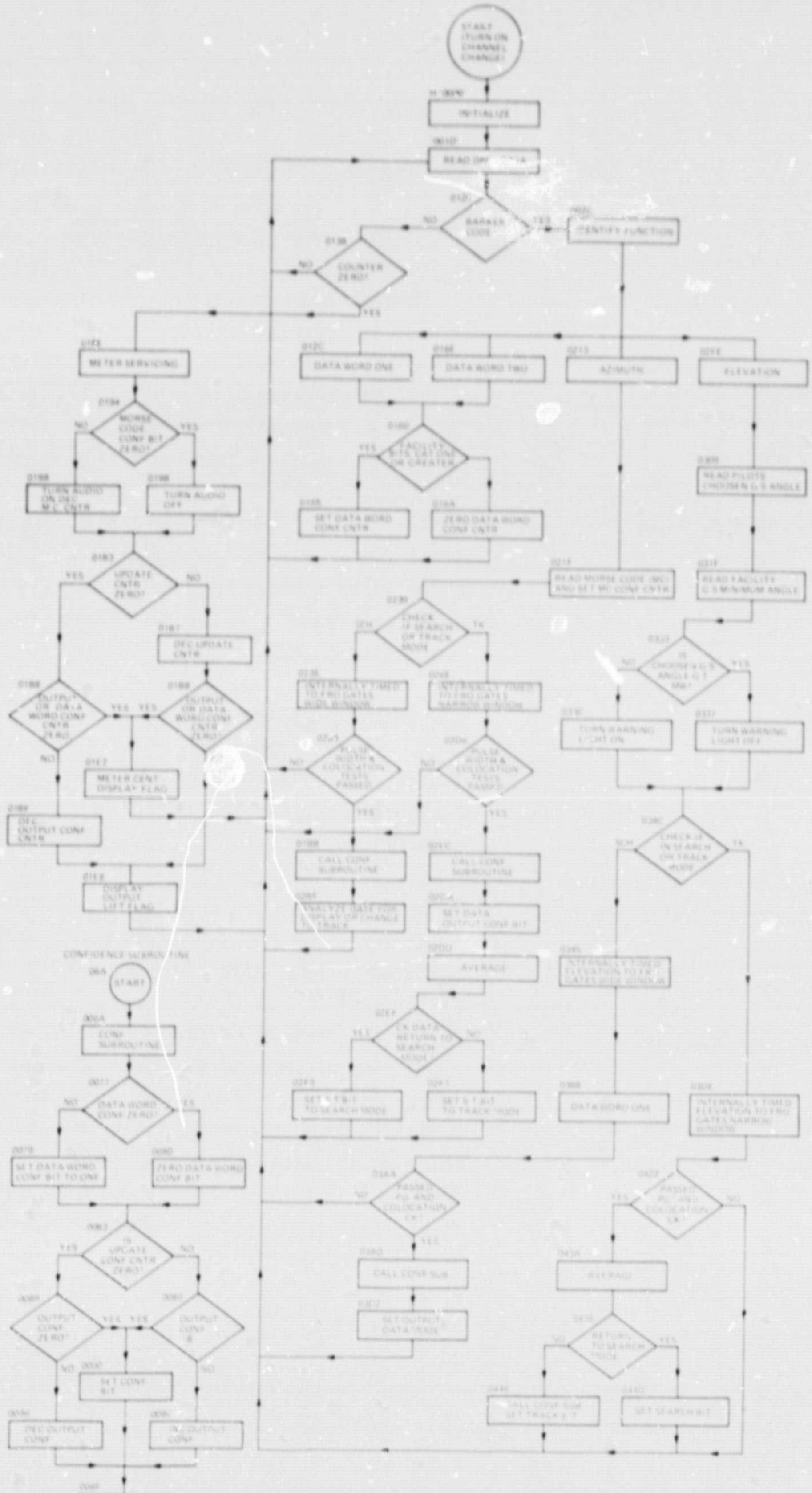


FIGURE 55. LCMLS PROCESSOR FLOW CHART

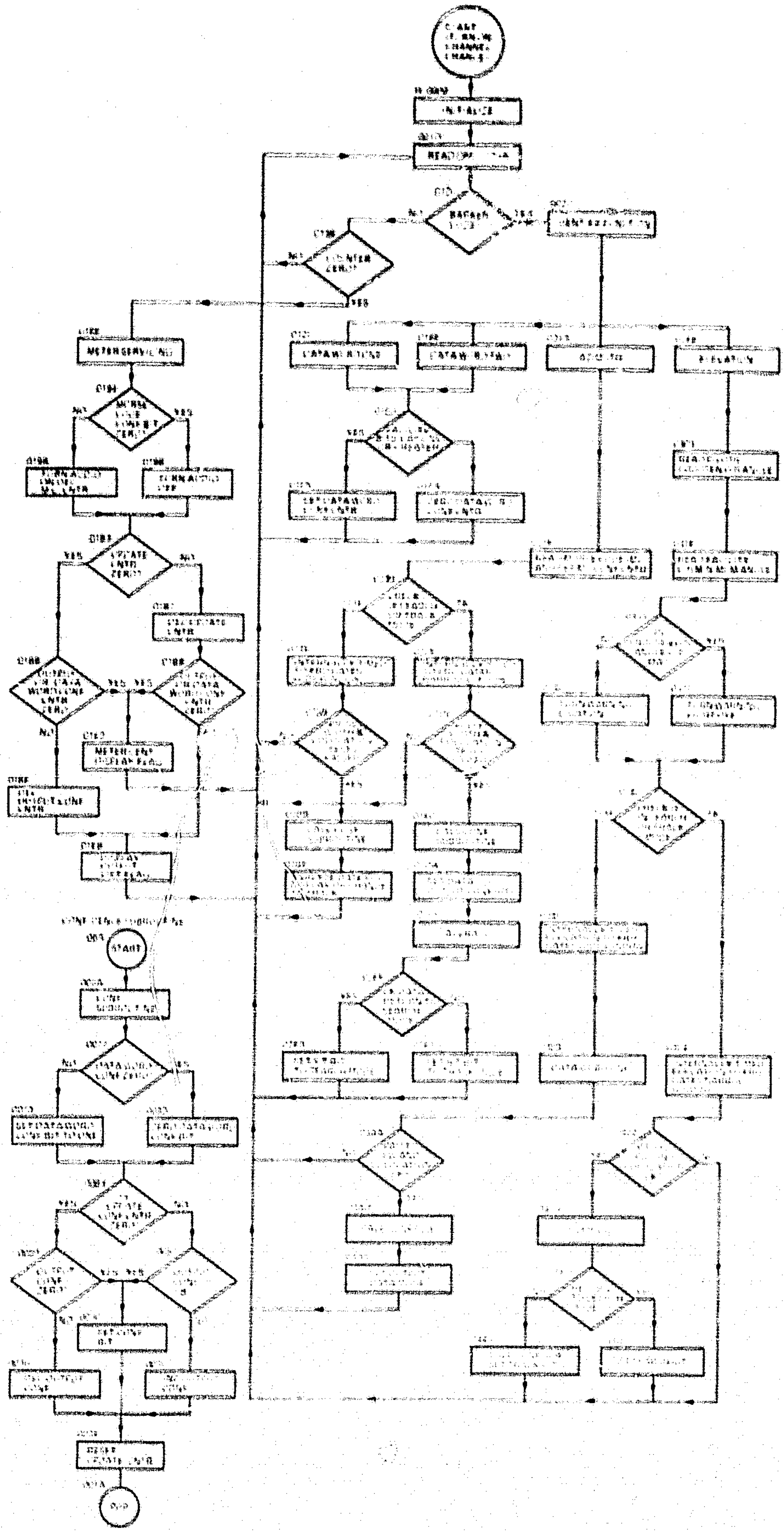


FIGURE 55. LCMLS PROCESSOR FLOW CHART

PROGRAM LISTING

```
C
                    *
                            ORG     H 0000
                    *
                    * MICROWAVE LANDING SYSTEM
                    *
                    * ASSEMBLED  12-30-77
                    *
                    *THE INITIALIZATION ROUTINE, UPON UNIT TURN ON AND
                    *UNIT CHANNEL CHANGES, DISABLES ALL INTERUPTS AND
                    *CLEARS ALL SCRATCH PAD REGISTERS, LOADS ADDRESS
                    *OF THE DPSK CLOCK SEARCH ROUTINE INTO KU, KL REG
                    *AND LOADS INTIAL LOCATION OF THE AVERAGING
                    *ROUTINE AZ AND EL STACK POINTERS
0000 1A             INTL    DI              *INITIALIZATION  INTERUPTS ARE
0001 20 3F                  LI      H 3F    DISABLED, ALL SCRATCH REGIS
0003 50                     LR      0,A     TERS ARE  CLEARED.
0004 40             CLR     LR      A,0     H 3F  LOADED INTO REG 0
0005 0B                     LR      ISAR,A  THIS BECOMES STARTS ADDRESS AND
0006 70                     CLR             IS PART OF A LOOP THAT DECREMENT
0007 5C                     LR      S,A     REG ZERO THUS CHANGING ISAR,
0008 30                     DS      0       POINTER LOCATION, EACH ADDRESS
0009 94 FA                  BNZ     CLR     IS LOADED WITH A CLEAR
000B B0                     OUTS    H 00    PORT ZERO OF CPU IS CLEARED
000C 64                     LISU    O 4     THE AVERAGING ROUTINE AZIMUTH
000D 68                     LISL    O 0     STACK POINTER  IS STORED AT REG
000E 20 18                  LI      H 18    O 40  POINTING TO STORAGE AREA
0010 5C                     LR      S,A     STARTING AT O 30  ( H 18 )
0011 67                     LISU    O 7     THE ELEVAATION POINTER IS STORED
0012 20 30                  LI      H 30    IN REG O 70  AND IT POINTS TO
0014 5C                     LR      S,A     STORAGE AREA  STARTING AT O 60
0015 20 1D                  LI      SCH,    *SCH IS A SUBROUTINE THAT
0017 05                     LR      KL,A    READS THE DPSK CLOCK TILL IT
0018 20 00                  LI      SCHP    CHANGES FROM POS TO NEG AT
001A 04                     LR      KU,A    WHICH POINT IT  READS DPSK DATA
001B 90 29                  BR      SERV    ROUTINE STORED IN KU & KL REGS
                    *THE  DPSK CLOCK SEARCH  SUBROUTINE MONITORS DPSK
                    *CLOCK (PORT 0,BIT 7,CPU) TILL IT GOES NEG
                    *AT WHICH TIME IT READS THE DPSK DATA (PORT 0,
                    *BIT 6) THIS DATA IS STORED IN REG 0 DATA
                    *CAN THEN BE READ IN 8 BIT CHUNKS
001D A0             SCH     IN      H 00    INITIALIZATION TO PK COMMAND
001E 91 FE                  BM      SCH     CALLS THIS ROUTINE
0020 13                     SL      1       PORT 0 BIT 7 CONNECTS TO DPSK
0021 81 05                  BP      ONE     CK BIT 6 TO DPSK DATA ( POS DUTY
0023 40                     LR      A,0     IS LONGER THAN NEG ) WHEN TRANSI
0024 13                     SL      1       IS DECTECTED TIME FOR RETURN
0025 50                     LR      0,A     IS LONG ENOUGH TO NOT RETURN
0026 1C                     POP             DURING NEG DUTY  AT SAME TIME DP
0027 40             ONE     LR      A,0     DATA IS READ AND STORED IN
0028 13                     SL      1       POS SENSE IN REG ZERO IF LOW IS
0029 1F                     INC             INPUT A ZERO IS  STORED, NEWEST
002A 50                     LR      0,A     IF A HIGH A ZERO IS STRD,NEWEST
002B 1C                     POP             DATA IS ENTERED AT LSB OLDEST SH
                    *THE IDENT ROUTINE IS ENTERED AFTER A BARKER CODE
                    *SEQUENCE IS FOUND, IT SEARCHES FOR AND IDENTIFIES
                    *FUNCTION WORDS FOR AZ, EL, DATA ONE, AND DATA TWO
002C 0C             IDENT   PK              * AFTER BARKER CODE IS FOUND
002D 0C              PK             FOUR DPSK CKS ARE DETECTED
002E 0C                     PK              AND ON CLOCK IS CONTENTS OF REG
002F 0C                     PK              ZERO (DPSK DATA) IS CHECKED FOR
0030 40                     LR      A,0     THE FOUR MSB  OF THE IDENT INCLD
0031 25 DC                  CI      H DC    THE LAST TWO  LSB OF BARKER CODE
0033 84 1D                  BZ      AZMT    (DC FOR AZIMUTH) (DF FOR ELEVA
0035 40                     LR      A,0     TION) IF NEITHER IS FOUND ONE
0036 25 DC                  CI      H DC    MORE CLOCK IS DETECTED AND THE
0038 84 0F                  BZ      ELV     LSB OF BARKER AND THE 4 MSB OF
003A 0C                     PK              THE DATA WORDS AND PARITY BITS
003B 40                     LR      A,0     ARE LOOKED FOR, (AA FOR DATA
003C 25 AA                  CI      H AA    WORD ONE) AND (AF FOR DATA
003E 84 0C                  BZ      DAT1    WORD TWO) IF NO FUNCTION IDENT
0040 40                     LR      A,0     IS MADE THERE IS
0041 25 AF                  CI      H AF    A RETURN TO THE BARKER
0043 84 0A                  BZ      DAT2    SEARCH ROUTINE)
0045 29 01 3D SERV          JMP     BRK1
0048 29 02 FE ELV           JMP     ELVN
004B 29 01 4E DAT1          JMP     D1RN
004E 29 01 6E DAT2          JMP     D2RN
0051 29 02 [illegible] AZMT JMP     AZM
                    *THE RESET SUBROUTINE RESETS ALL DATA COUNTERS (FOR
                    *MEASURING TIME OF PULSES AND PULSE WIDTH, THE
                    *DURATION OF THE RESET ALSO TIMES OUT MIDSCAN OF
                    *EL SEARCH MODE) THEN SET BACK TO NORMAL STATE
0054 20 1F          RESET   LI      H 1F    *THIS SUBROUTINE SETS OUTPUT
0056 B0                     OUTS    H 00    OF PORT 0 BIT 5 HIGH  CAUSING
0057 20 FA                  LI      H FA    THE PULSEWIDTH COUNTER, THE
0059 1F             LOOP    INC             DATA COUNTERS, THE LATCH AND THE
005A 94 FE                  BNZ     LOOP    ONE SHOTS TO RESET, DURATION OF
005C 20 3F                  LI      H 3F    RESET IS TIMED BY THE
005E B0                     OUTS    H 00    COUNTER CALLED LOOP AFTER WHICH
005F 1C                     POP             THE RESET HIGH IS RESET LOW
                    *THE STROBE SUBROUTINE OUTPUTS A DOUBLE PULSE
                    *THAT STROBES PW DATA FROM PW COUNTER THROUGH
                    *THE DATA COUNTER THROUGH THE LATCH TO BE
                    *READ AT DATA INPUT PORT (PORT 1 BITS 0-7 CPU)
                    *THE PREPROSSERS SCD IS ALSO RESET
0060 20 37          STROBE  LI      H 37    *THIS SUBROUTINE SETS PORT 0 BIT
0062 B0                     OUTS    H 00    3 HIGH  RESETTING THE SCD AND
0063 20 3F                  LI      H 3F    STROBING PW THROUGH LATCH
0065 B0                     OUTS    H 00    OFF AND ON AGAIN FOR 2ND STRO
0066 20 37                  LI      H 37    BEE AND HELD HIGH TILL READ
0068 B0                     OUTS    H 00    CONTENTS OF PW COUNTER ARE THEN
0069 1C                     POP             READ
```

PROGRAM LISTING

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                    *THE CONFIDENCE SUBROUTINE IS ONLY ENTERED IF
                    *THERE WERE COLOCATED PULSES OF PROPER PULSE
                    *WIDTH.  FIRST DATA WORD CONFIDENCE IS CHECKED
                    *DATA WORD BIT OF OUTPUT CONF REG IS SET ACCORD
                    *INGLY CONF DEPENDS ON STATUS OF GEN FAC
                    *CATEGORY BITS OF DATA WORD.  NEXT UPDATE
                    *CONF IS CHECKED AND OUTPUT CONF COUNTER IS
                    *INC OR DEC ACCORDINGLY IF INC TO 3 THEN
                    *THE DATA OUTPUT BIT IS SET. BOTH DATA WORD
                    *AND DATA OUTPUT BITS MUST BE HIGH TO OUTPUT
                    *ANY DATA  LAST THE UPDATE CONF COUNTER IS RESET
006A 20 35   CONAZ   LI     H'35   *CONFIDENCE SUB MAY BE ENTERED
006C 90 03           BR     CONF   BY AZ OR EL. REG 2 IS LOADED
006E 20 15   CONEL   LI     H'15   WITH EACH SEP UPDATE CONF
0070 53      CONF    LR     3,A    IDENCE AZ IS THREE TIMES GREATER
0071 6B              LISL   3      THEN EL BECAUSE IT OCCURS 3 TIM
0072 2A              CLR           LESS. POINTER IS SET AT DATA
0073 CC              AS     S      WORD CONFIDENCE (AZ 0 43 : EL 0
0074 84 09           BZ     STEL   23) IF THIS COUNTER IS ZERO
0076 3C              DS     S      THERE IS NO DATA WORD CONFIDENCE
0077 6D              LISL   5      BIT  EVEN OF OUTPUT CONF
0078 4C              LR     A,S    REGISTER (AZ 45 : EL 25) IS SET
0079 22 00           OI     H'00   TO ZERO THUS DISABLING ANY OUT
007B 5E              LR     D,A    PUT OF DAT DURING METER SERVICE
007C 90 06           BR     CPI    SUB IF DATA WORD COUNTER IS
007E 6D      STEL    LISL   5      NOT ZERO THAN DATA WORD BIT 7
007F 4C              LR     A,S    OF OUTPUT CONF REGISTER IS SET
0080 21 7F           NI     H'7F   HIGH (OI H'80) EITHER CASE
0082 5E      LR      D,A    THE POINTER WAS DEC TO
0083 70      CPI     CLR           POINT AT UPDATE CONF COUNTER
0084 CD              AS     I      WHICH IS INCREMENTED AFTER COLO
0085 84 10           BZ     DEC    CATED DATA AND CHECKED FOR ZERO
0087 4C              LR     A,S    POITR SET TO OUTPUT CONF
0088 15              SL     4      4 LSB ARE CHECKED IF GREATER THA
0089 91 06           BM     SET    2(IE, BIT 6 HIGH) IF NOT, 3
008B 4C              LR     A,S    THEN COUNTER IS INC BY ONE
008C 1F              INC           BIT IF GREATER GO TO SET
008D 5E              LR     D,A    AFTER INC COUNTER  POINTER
008E 90 10           BR     PRO    IS SET TO POINT AT UPDATE(PRO)
0090 4C      SET     LR     A,S    SET**THIS SETS BIT 6 HIGH
0091 22 40           OI     H'40 OF OUTPUT CONF REGISTER A
0093 5E              LR     D,A    NECESSITY TO OUTPUT DATA
0094 90 0A           BR     PRO    POINTER RESET TO UPDATE REG
0096 4C      DEC     LR     A,S    IF UPDATE COUNTER WERE ZERO
0097 15              SL     4      THEN OUTPUT CONF CNTR IS
0098 94 14           BNZ    OFST   DECREMENTED TO ZERO
009A 3C              DS     D      TO SET BIT 6 HIGH IT IS ONLY
009B 90 0?           BR     PRO    AFTER QUALIFIED DATA AT PRO
009D 70      OFST    CLR           3 TIMES OR (OFST) WILL
009E 5E              LR     D,A    CLEAR ALL CONF COUNTER
009F 42      PRO     LR     A,2    AZ AND COLOCATION WERE PASSED
00A0 5D              LR     I,A    SO THE UPDATE CNTR IS RESET
00A1 1C              POP
                    *THE DURATION SUBROUTINE TIMES THE DURATION OF
                    *AZIMUT SEARCH MODE GATE
00A2 70      DURAT   CLR           *THIS SUBROUTINE IS THE TIMEER
00A3 0F      DRT     LR     DC,Q   FOR THE AZIMUTH TO AND PRO CHAN
00A4 1F              INC           ENABLE . IT IS IN TWO SECTIONS FI
00A5 94 FE           BNZ    DRT    COUNTER DELAYED BY THE LOW
00A7 20 FF           LI     H'FF   DATA REG . SECOND COMMAND THE SECOND
00A9 1F      FLUX    INC           COUNTER FINE TUNES THE DURATION
00AA 94 FE           BNZ    FLUX   TO AND PRO CHAN ARE EQUAL IN
00AC 1C              POP    LENGTH OF ENABLE
                    *THE COLOCATION SUBROUTINE CHECKS THAT CENTER
                    *OF CENTROID OF BOTH SCAN ARE COLOCATED
                    *AND THAT THE PW IS WITHIN SPEC AND IF SO THE
                    *DATA IS ACCEPTED
00AD 45      AZPW    LR     A,5    *PW CLOCK IS 200 KHZ BUT AZ SCAN
00AE 14              SR     4      DATA CLOCK IS 50 KHZ THE PW IS A
00AF 12              SR     1      TO BE DIVIDED IN HALF TO
00B0 53              LR     3,A    TO REDUCE TO THE CENTER OF THE
00B1 42              LR     A,2    THE PULSE IS DIVIDED BY 32
00B2 14              SR     4      AND THIS NUMBER IS STORED SEPER
00B3 12              SR     1      ATELY FROM UNREDUCED PW DATA
00B4 06              LR     QU,A   THAT WILL BE USED FOR WIDTH CK
00B5 90 1B           BR     COLO   DIVIDED DATA USED FOR COLO CK
00B7 45      AZRW    LR     A,5    AZ   TRACK MODE IS 50 KHZ AN
00B8 12              SR     1      PW CLOCK IS DIVIDED BY TWO
00B9 12              SR     1      ONCE TO SYNCRONIZE AND AGAIN
00BA 53              LR     3,A    TO HALVE THE PW
00BB 42              LR     A,2
00BC 12              SR     1
00BD 12              SR     1
00BE 06              LR     QU,A
00BF 90 11           BR     COLO
00C1 45      EL PW   LR     A,5    THE ELEVATION SEARCH DATA CLOCK
00C2 12              SR     1      IS 25KHZ SO THE PW CLOCK IS
00C3 12              SR     1      DIVIDED BY 8 (BY FOUR TO
00C4 12              SR     1      SYNCRONIZE AND BY TWO
00C5 53              LR     3,A    TO DIVIDE PW
00C6 42              LR     A,2
00C7 12              SR     1
00C8 12              SR     1
00C9 12              SR     1
00CA 06              LR     QU,A
00CB 90 05           BR     COLO
00CD 45      ELTRW   LR     A,5    THE ELEVATION TRACK MODE
00CE 53              LR     3,A    IS 1.6 MHZ SO EL PW IS ALREADY
00CF 42              LR     A,2    1/2 PW AND IS LEFT UNCHANGED
00D0 06              LR     QU,A
00D1 44      COLO    LR     A,4    **CHECK COLOCATION  TO(UP
00D2 CA              AS     A      DOWN) DATA HAS 1/2 OF
00D3 54              LR     4,A    ADDED TO ITT
00D4 A2              LR     A,QU   ONE HALF OF PRO(OR UP) PW
00D5 10              COM           IS 2'S COMP SUBTRACTED FROM
00D6 1F              INC           PRO (OR UP) DATA
```

PROGRAM LISTING

```
00D7 C6                AS     6
00D8 56                LR     6,A       FRO DATA MINUS 1/2 OF THE PW
00D9 18                COM              IS SUBTRACTED FROM  THE TO DATA
00DA 1F                INC              (+ 1/2 OF PW) THEN SHIFTED RIGHT
00DB C4                AS     4         FOUR TO CK IF CENTER OF CENTROID
00DC 82 05             BC     COCO      IS WITHIN 16 DATA CLOCKS
00DE 44                LR     A,4       NO CARRY INDICATES THAT TO DATA
00DF 18                COM              IS LARGER THAN FRO IN WHICH
00E0 1F                INC              CASE THE TO DATA + 1/2 OF PW
00E1 C6                AS     6         IS SUB FROM FRO -1/2  PW AND
00E2 14         COCO   SR     4         CHECKED IF DIFFERENCE IS
00E3 94 59             BNZ    BRK1      16 CKS
00E5 47         PW     LR     A,7       *PULSEWIDTH CHECK BOTH THE
00E6 25 19             CI     H'19'     TO AND THE FRO PULSES
00E8 82 54             BC     BRK1      40 MICRO  SEC WIDE MIN
00EA 25 C4             CI     H'C4'     AND 250 MICRO SEC WIDE MAX
00EC 92 50             BNC    BRK1
00EE 45                LR     A,5       TO PULSE WIDTH CK SAME AS FRO
00EF 25 19             CI     H'19'
00F1 82 4B             BC     BRK1
00F3 25 C4             CI     H'C4'
00F5 92 47             BNC    BRK1
00F7 44         DAAVG  LR     A,4       *AVERAGE TO AND FRO DATA
00F8 C6                AS     6         TO DATA +1/2 OF PW IS ADDED
00F9 92 04             BC     DIVD      TO FRO DATA -1/2 OF PW AND
00FB 12                SR     1         DIVIDED BY TWO IF THE SUM HAS
00FC 90 04             BR     TRO       A CARRY THE CARRY IS
00FE 12         DIVD   SR     1         ACCOUNTED FOR BY THE
00FF 24 80             AI     H'80' AI H'80' BYPASS
0101 54         TRO    LR     4,A
0102 1C                POP
                *THE AVERAGING SUBROUTINE SAVES EIGHT PREVIOUS
                *DATA THAT ARE SAVED IN A FILO STACK IN
                *SCRATCH PAD WITH THE SUM OF THE EIGHT DATAS
                *ALSO SAVED. NEW DATA CONTINUALLY REPLACES
                *OLDEST DATA IN THE STACK AND THE SUM IS
                *CONTINUALLY ADDED TO BY NEW DATA AND SUB-
                *TRACTED FROM BY THE OLDEST. THE SUM IS
                *DIVIDED BY  EIGHT FOR OUTPUT TO THE METER
0103 69         AVRG   LISL   O'0'      **AVERAGING SUBROUTINE POINT FIR
0104 4C                LR     A,S       TO STACK POINTER THEN LOAD ISAR
0105 0B                LR     IS,A      SO IT NOW POINTS TO LOC OF OLDST
0106 4C                LR     A,S       LOAD OLDEST DATA INTO REG 7 AND
0107 57                LR     7,A       TAKE NEWEST DATA AND LOAD INTO
0108 44                LR     A,4       THE STACK AND INC POINTER TO
0109 5D                LR     I,A       NEXT LOCATION (AUTO LOOP) NEW
010A 0A                LR     A,IS      POINTER LOCATION IS STORED BACK
010B 68                LISL   O'0'      INTO THE STACK POINTER REGISTER
010C 5D                LR     I,A       ISAR INC TO DATA LOWER BYTE
010D 44                LR     A,4       NEWEST DATA IS ADDED TO SUMS
010E CC                AS     S         LOWEST BYTEPOINTER IS INCREMENTE
010F 5D                LR     I,A       AND ANY CARRY IS ADDED TO
0110 70                CLR              UPPER BYTE AND THE POINTER DEC
0111 19                LNK              TO LOWER BYTE
0112 CC                AS     S
0113 5E                LR     D,A
0114 47                LR     A,7       OLDEST DATA IS SUBTRACTED (ZERO
0115 18                COM              IS DETECTED IF ZERO NO FURT OPER
0116 1F                INC              MADE TO NOT DISORIENT CARRY WITH
0117 84 09             BZ     FWEN      ZERO) FROM LOWER BYTE OF DATA
0119 CC                AS     S
011A 92 05             BC     NOCA      NO CARRY INDICATES THAT A
011C 5D                LR     I,A        BORROW IS TO BE MADE ON THE
011D 3C                DS     S         UPPER BYTE
011E 90 02             BR     FWEN
0120 5D         NOCA   LR     I,A       IF SO DEC UPPER BYTE BY ONE
0121 4E         FWEN   LR     A,D       ***DATA IS PREPARED FOR OUTPUT
0122 15                SL     4         UPPER BYTE SHIFTED LEFT FIVE
0123 13                SL     1         IS ADDED TO THE LOWER BYTE
0124 59                LR     9,A       SHIFTED RIGHT THREE THIS IS AN
0125 4C                LR     A,S       EQUIVALENT DIVISION BY EIGHT
0126 12                SR     1         THIS AVERAGED OUTPUT REDUCES
0127 12                SR     1         THE EFFECTS OF JITTER
0128 12                SR     1
0129 C9                AS     9
012A 59                LR     9,A
012B 1C                POP
                *THE BARKER CODE SEARCH ROUTINE CONTINUALLY
                *LOOKS FOR A VALID BARKER CODE IF NONE IS FOUND
                *TIMERS TIME OUT AND METER SEVICE IS CALLED
                *IF A VALID BARKER IS FOUND THEN THERE IS
                *A JUMP TO IDENT TO IDENTIFY THE FOLLOWING
                *FUNCTION
012C 0C         BRK3   PK                  **THIS ROUTINE SEARCHES FOR BARK
012D 40                LR     A,0          CODE'S LAST FOUR BITS ( TO PREVE
012E 21 0F             NI     H'0F'        INTIAL LOCKON MISSES
0130 23 0D             XI     H'0D'                     IT CONSISTS OF T
0132 84 10             BZ     ID2          RUN OUT CALLS METER SERVICING IF
0134 31                DS     1            BARKER IS FOUND THEN IDENT ROUTI
0135 94 F6             BNZ    BRK3         FOR A FUNCTION WORD IF ENTERED
0137 20 FF      BRK2   LI     H'FF'        AT BRK1 TIMERS INITIALIZE AND
0139 51                LR     1,A          METER SER IS IMEDIATE ALL OTHER
013A 33                DS     3            ENTRIES GIVE A RANDOM COUNTDOWN
013B 94 F0             BNZ    BRK3         METER SERVV
013D 20 03      BRK1   LI     H'03'
013F 53                LR     3,A
0140 29 01 3E          JMP    METS
0143 29 00 2C   ID2    JMP    IDENT
0146 20 15      BRK5   LI     H'15'        SHORT COUNTDOWN OF DETERMINED
0148 5D                LR     I,A          LENGTH
0149 20 01             LI     H'01'
014B 53                LR     3,A
014C 90 DF             BR     BRK3
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PROGRAM LISTING

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                   *THE DATA WORD ONE ROUTINE VARIFIES PARITY
                   *BITS OF FUNCTION WORD AND LOOKS FOR THE
                   *THE STATUS OF THE CATEGORY BITS IF BOTH ARE
                   *NOT ZERO THE DATA WORD CONF REG IS INC
014E 0C       D1RU   PK            **DATA WORD ONE ROUTINE
014F 40              LR     A,0    CHECK FUNCTION ID AND PARITY BIT
0150 25 54           CI     H'54   COUNT THE DPSK CLOCKS AND
0152 84 03           BZ     DONE   THEN CHECK GROUND FACILITY
0154 90 E0           BR     BRK1   CATEGORY STATUS BITS
0156 0C       DONE   PK            DPSK CLOCK 15
0157 20 09           LI     H'09   THIS COUNTER COUNTS DPSK CLOCKS
0159 52              LR     2,A    TILL REG 0 CONTAINS THE FACILITY
015A 64              LISU   O'4     BITS AS 2 LSD
015B 6B              LISL   O'3
015C 0C       LOC    PK
015D 32              DS     2
015E 94 FD           BNZ    LOC
0160 40              LR     A,0    CHECK IF BOTH BITS ARE ZERO
0161 21 03           NI     H'03   INDICATING CATAGORY ZERO
0163 84 06           BZ     UNFG   CONF ON ONLY CAT 1 OR ABOVE
0165 20 20           LI     H'20   ONE OR ABOVE LOAD DATA WORD
0167 5C              LR     C,A    CONFIDENCE COUNTERR
0168 90 D4           BR     BRK1
016A 70       UNFG   CLR           IF ZERO CLEAR DATA WORD CONF
016B 5C              LR     C,A    COUNTER
016C 90 D0           BR     BRK1
                   *THE DATA WORD TWO ROUTINE VERFIES PARITY
                   *BITS OF THE FUNCTION WORD AND LOOKS FOR
                   *STATUS OF THE CATEGORY BITS, IF BOTH ARE
                   *NOT ZERO THE DATA WORD CONF REG IS INC
016E 0C       D2RU   PK            ***DATA WORD TWO
016F 40              LR     A,0    CHECKS DONE SAME AS DAT ONE
0170 25 5E           CI     H'5E   CHECK FUNCTION AND PARITY
0172 84 04           BZ     ADDN
0174 90 C8           BR     BRK1
0176 0C       ADDN   PK
0177 20 10           LI     H'10
0179 52              LR     2,A
017A 67              LISU   O'7
017B 6B              LISL   O'3
017C 0C       ALOC   PK
017D 32              DS     2
017E 94 FD           BNZ    ALOC
0180 40              LR     A,0
0181 21 03           NI     H'03   CHECK FACILITY BITS
0183 84 06           BZ     ANNF
0185 20 20           LI     H'20   CAT ONE OR GREATER SET DATA WORD
0187 5C              LR     C,A    TWO CONF COUNTER
0188 90 B4           BR     BRK1
018A 70       ANNF   CLR           CAT ZERO, CLEAR CONF COUNTER
018B 5C              LR     C,A
018C 90 B0           BR     BRK1
                   *THE METER SERVICE ROUTINE FIRST CHECKS CONF
                   *BEFOR OUTPUTING ANY DATA NO CONF ONLY
                   *METER CENTER AND FLAG IS OUTPUT
018E 64       METS   LISU   O'4    **METER SERVICE ROUTINE
018F 6F              LISL   O'7    POINT AT MORSE CODE CON CNTR
0190 70              CLR
0191 CC              AS     S
0192 94 05           BNZ    MOUT
0194 20 03           LI     H'03   M.C. CONF ZERO NO OUTPUT TURNS
0196 90 04           BR     DIFA   AUDIO OFF SET AS FUNCTIONS
0198 A4       MOUT   IN     H'04   M.C. CONF NOT ZERO MODIFY NO
0199 21 0?           NI     H'0?   OUTPUT SO IT DOES NOT CHANGE
019B 5?       DIFA   LR     2,A    MORSE CODE DATA
019C 20 F?           LI     H'F?
019E C?              A?     ?
019F 5?              LR     9,A    STORE MORSE MODIFIED
01A0 8?              LR     A,?A   CALCULATE OUTPUT DATA+IF ANY
01A1 0?              LR     0U,A   AS DATA STORED FOR OUTPUT
01A2 20 E9           LI     H'E9   THIS NUMBER IS THE TIME ALLOWED
01A4 0?              LR     0L,A   FOR METER SETTLING BETWEEN MO
01A5 6C              LISL   O'4    CHANGES, POINT TO M? UPDATE CONF
01A6 28 01 B?        PI     MESR
01A9 67              LISU   O'7    MOVE POINTER TO EL UPDATE
01AA 6C              LISL   O'4    CONFIDENCE COUNTER
01AB 4D              LR     A,D    STORE CALCULATED EL DATA
01AC 0?              LR     0U,A   FOR OUTPUT
01AD 28 01 B3        PI     MESR
01B0 29 01 ??        JMP    BRK2   RETURN TO BASKER SEARCH
01B3 70       MESR   CLR           **METER SERVICE OUTPUT SUBROUTIN
01B4 CC              AS     S      CHECK IF UPDATE CONF IS ZERO IF
01B5 84 0?           BZ     DECT   SO TO SITENTY AND CLR CONF COUNT
01B7 3?              DS     I      IF NOT ZERO DEC UPDATE CONF
01B8 20 40           LI     H'40   AND ADD TO OUTPUT CONF IF BOTH
01BA CE              AS     D      DATA WORD CONF BIT ? AND OUTPUT
01BB 92 ?6           BNC    CENT   BIT 6 ARE HIGH THEN A CARRY IS G
01BD 90 0?           BR     DAOT   PROCEED TO DAOT IF NOT ENOUGH
01BF 70       DECT   CLR           CONF TO OUTPUT DATA
01C0 5?              LR     I,A    CLEAR BOTH UPDATE AND OUTPUT CON
01C1 5?              LR     ?,A
01C2 90 1F           BR     CENT
01C4 6E       DAOT   LISL   O'6    POINT TO DATA OUTPUT REG TO DE
01C5 70              CLR          TERMINE IF FULL LFT,RIGHT, OR SE
01C6 59              LR     9,A    OR THAT CALCULATED DATA IS TO BE
01C7 4?              LR     A,?    REG 9 CLRED TO STP FALSE OUTPUT
01C8 24 20           AI     H'20   IF BITS 7,6,5, ARE HIGH DISPLAY
01CA 82 0B           BC     LFT    FULL LEFT DIFLECTION
01CC 4C              LR     A,S
01CD 24 40           AI     H'40   IF BITS 7,6 ARE HIGH DISPLAY
01CF 82 0B           BC     RGT    FULL RIGHT DIFLECTION
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PROGRAM LISTING

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01D1 4C                LR    A,S
01D2 24 80             AI    H 80     IF ONLY BIT 7 IS HIGH DISPLAY
01D4 82 13             BC    DATE     CALCULATED DATAA
01D6 90 0B             BR    CENT     BITS 7,6,5 LOW DISPLAY CENTER
01D8 20 FF      LFT    LI    H FF     REG QU WILL HLD OUTPUT DATA
01DA 06                LR    QU,A     METER COMMON 7F, DIFFRENTIAL
01DB 90 0C             BR    DATE     FROM 7F DETERMINES MEETER DIFLEC
01DD 20 01      RGT    LI    H 01     TION
01DF 06                LR    QU,A
01E0 90 07             BR    DATE
01E2 20 7F      CENT   LI    H 7F
01E4 06                LR    QU,A
01E5 20 FF             LI    H FF     DISPLAY THE FLAG,OUTPUT
01E7 59                LR    9,A      OVER WRITTEN BY CONF DATA ONLY
01E8 20 7F      DATE   LI    H 7F     METER COMMON DATA
01EA 27 05             OUT   H 05
01EC 48                LR    A,8      METER COMMON MUX
01ED 38                DS    8
01EE 27 04             OUT   H 04
01F0 03                LR    A,QL     METER SETTLING TIME
01F1 1F         SET2   INC
01F2 94 FE             BNZ   SET2
01F4 70                CLR            TURNS MUX OUTPUT OFF
01F5 C7                AS    7        MODIFIED BY MORSE CODE STATUS
01F6 27 04             OUT   H 04
01F8 02                LR    A,QU     METER DATA OUT
01F9 27 05             OUT   H 05
01FB 49                LR    A,8      METER DETA MUX
01FC 39                DS    9
01FD 27 04             OUT   H 04
01FF 70                CLR            MUX TURNED OFF
0200 C7                AS    7        MODIFIED BY MORSE CODE
0201 27 04             OUT   H 04
0203 49                LR    A,9      FLAG STATUS DATA
0204 27 05             OUT   H 05
0206 49                LR    A,9      FLAG STATUS MUX
0207 39                DS    9
0208 27 04             OUT   H 04
020A 03                LR    A,QL     METER SETTLING TIME
020B 1F         SET5   INC
020C 94 FE             BNZ   SET5
020E 70                CLR            MUX TURNED OFF
020F C7                AS    7        MODIFIED BY MORSE CODE STATUS
0210 27 04             OUT   H 04
0212 1C                POP
                *AZIMUTH ROUTINE
0213 0C         AZM    PK             ****AZIMUTH ROUTINE
0214 0C                PK             COUNT TWO DRSF CLOCKS (15-16)
0215 40                LR    A,0      CHECK PARITY BITS
0216 25 40             CI    H 40
0218 84 04             BZ    AZIN
021A 29 01 3D   CBRA   JMP   BRK1
021D 0C         AZIN   PK             COUNT 4 DRSF CLOCKS (17-20)
021E 0C                PK
021F 64                LISU  O 4      POINTER TO MORSE CODE CONF CNTR
0220 6F                LISL  O 7
0221 0C                PK
0222 20 20             LI    H 20     VALID ID LOAD MORSE CODE CONF
0224 5C                LR    S,A
0225 0C                PK             DRSF CLOCK 20
0226 40                LR    A,0      CHECK DRSF FOR GAND FACILITY M.C
0227 18                COM            BIT,COMPLIMENT SO IT IS OUTPUT
0228 21 08             NI    H 08   IN PROPER POLARITY
022A 27 04             OUT   H 04
022C 0C                PK
022D 20 37             LI    H 37     RESET CCD USING RE STROBE
022F B0                OUTS  H 00
0230 20 D4             LI    H D4     TIMER FOR TURNING CCD RESERT OFF
0232 1F         CLOCK  INC
0233 94 FE             BNZ   CLOCK
0235 20 1F             LI    H 1F     RESET DATA COUNTERS
0237 B0                OUTS  H 00
0238 6D                LISL  O 5      POINT TO OUTPUT CONF REG, BIT
0239 4C                LR    A,S      5 OF THIS REGISTER WHEN HIGH IND
023A 21 20             NI    H 20     CATES TK MODE IF LOW SCH MD
023C 94 31             BNZ   TRACK
                *AZIMUTH SEARCH MODE ROUTINE
023E 20 B0             LI    H B0     **SEARCH MODE ROUTINE, TIME
0240 1F         TTS    INC            TILL BEGINNING OF ENABLE
0241 94 FE             BNZ   TTS
0243 20 2C             LI    H 2C     ENABLE 40 KHZ CLOCK
0245 B0                OUTS  H 00
0246 28 00 A2          PI    DURAT    TIMES LENGTH OF ENABLE WINDOW
0249 70                CLR            INPUT PORT
024A B1                OUTS  H 01
024B A1                INS   H 01     READ INPUT DATA
024C 54                LR    4,A      STORE TO SCAN DATA
024D 28 00 6D          PI    STROBE   STROBE FM THROUGH LATCH
0250 A1                IN    H 01     READ TO FM
0251 55                LR    5,A      STORE TO FM DATA
0252 20 95             LI    H 95     TIMES OUT MIDSCAN
0254 1F         CLO2   INC
0255 94 FE             BNZ   CLO2
0257 20 1F             LI    H 1F     RESET DATA COUNTER
0259 B0                OUTS  H 00
025A 20 2E             LI    H 2E     ENABLE FRD (INVERT T C LINE
025C B0                OUTS  H 00
025D 28 00 A2          PI    DURAT    DURATION OF WINDOW
0260 70                CLR            CLR DATA PORT
0261 B1                OUTS  H 01
0262 56                LR    6,A      STORE FRD SCAN DATA
0263 28 00 6D          PI    STROBE   STROBE FM THRU LATCH
0266 A1                INS   H 01     READ FRD FM
0267 57                LR    7,A      STORE FRD FM DATA
0268 28 00 54          PI    RESET    RESET ALL DATA COUNTERS
026B 6C                LISL  O 4      POINT TO UPDATE CONF CNTR
026C 90 4B             BR    SCHMD
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PROGRAM LISTING

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                        *AZIMUTH TRACK MODE ROUTINE
026E 20 00      TRACK   LI      H 00      ***TRACK MODE ROUTINE, THIS AND
0270 1F         CLD3    INC               NEXT COUNTER DETERMINES START O
0271 94 FE              BNZ     CLD3      TRACK WINDOW. TRACK WINDOW IS
0273 20 00              LI      H 00      TWICE DATA COUNTER LENGTH THUS
0275 1F         CLD4    INC               TRACK MODE HAS FRONT PORCH
0276 94 FE              BNZ     CLD4      ALLOWING COVERAGE OF PULSES THAT
0278 20 3C              LI      H 3C      WOULD OTHERWISE OVER LAP WINDOW
027A B0                 OUTS    H 00      *ENABLE OUTPUT
027B 20 24              LI      H 24      ENABLE DURATION
027D 1F         CLD5    INC
027E 94 FE              BNZ     CLD5
0280 20 3D              LI      H 3D      TURNS THE TO SCAN ENABLE OFF
0282 B0                 OUTS    H 00
0283 70                 CLR               CLEAR THE DATA INPUT PORT
0284 B1                 OUTS    H 01
0285 A1                 INS     H 01      READ TO SCAN DATA
0286 54                 LR      4,A       STORE DATA
0287 20 00              LI      H 00      THIS COUNTER WITH TIME EXTENDER
0289 10         CLD6    LR                DELAY DELAYS THE STROBE
028A 1F                 INC               WHICH IS ALSO THE CCD RESET TILL
028B 94 FD              BNZ     CLD6      SCAN TO PREVENT CUT OFF OF PW
028D 28 00 6A           PI                PW ULSE AND CCD RESET
0290 A1                 INS     H 01      READ TO PW
0291 55                 LR      5,A       STORE TO PW DATA
0292 20 1F              LI      H 1F      MASTER RESET ALL DATA COUNTERS
0294 B0                 OUTS    H 00
0295 20 40              LI      H 40      THIS COUNTER TIMES OUT DURATION
0297 1F         CLD7    INC               OF MID SCAN
0298 94 FE              BNZ     CLD7
029A 20 3F              LI      H 3F      FRO SCAN ENABLE
029C B0                 OUTS    H 00
029D 20 24              LI      H 24      THIS COUNTER TIMES
029F 1F         CLD8    INC               DURATION OF FRO SCAN WITH
02A0 94 FE              BNZ     CLD8      FRONT PORCHES
02A2 20 3F              LI      H 3F      TURNS OFF FRO SCAN
02A4 B0                 OUTS    H 00
02A5 70                 CLR               CLEAR DATA INPUT PORT
02A6 B1                 OUTS    H 01
02A7 A1                 INS     H 01      READ FRO SCAN DATA
02A8 56                 LR      6,A       STORE DATA
02A9 20 22              LI      H 22      THIS COUNTER DELAYS THE PE=
02AB 1F         CLD9    INC               CCD RESET SO IT WON T INTER
02AC 94 FE              BNZ     CLD9      FERE WITH WIDE PULSES
02AE 28 00 6F           PI      STROBE    STROBE PW AND RESET CCD
02B1 A1                 INS     H 01      READ PW
02B2 57                 LR      7,A       STORE FRO PW
02B3 28 00 54           PI      RESET     MASTER RESET ALL DATA COUNTERS
02B6 90 1F              BR      TRCK
                        *SEARCH MODE CONT
02B8 28 00 AD   SCAND   PI      ASPW      CHECK PW AND COLOCATION
02BB 28 00 6A           PI      COMM2     IN CONE CHIR *FASTER COLO*
02BE 6E                 LISL    O 6       POINT TO OUTPUT DATA REGISTER
02BF 44                 LR      A,4       READ DATA TO DETERMINE IF IN
02C0 25 20              LI      H 20      LEFT OR RIGHT QUADRANT OR IN
02C2 82 0?              BC      LEFT      CENTER QUADRANTS. IF IN CENTER
02C4 44                 LR      A,4       CHANGE TO TRACK MODE (TK2)
02C5 25 05              CI      H 05      USE IT FROM COMM2 POINTING
02C7 ?? 04              BM      RIGHT     TO UPDATE CONE REG 11
02C9 90 ??              BR      TK2
02CB 20 C0      LEFT    LI      H C0      SET FULL LEFT BITS IN
02CD 5C                 LR      S,A       OUTPUT DATA REGISTER
02CE 90 ??              BR      TK2
02D0 6B                 LISL    O 6
02D1 20 E0      RIGHT   LI      H E0      SET FULL RIGHT BITS IN
02D3 5C                 LR      S,A       IN OUTPUT DATA REGISTER
02D4 90 1F              BR      TK2
                        *TRACK MODE CONT
02D6 28 00 B? TRCK      PI      ATPW      ***TRACK MODE - CHECK COLOCATION
02D9 6E                 LISL    O 6       FASTER COLOCATION SET DATA
02DA 20 ??              LI      H ??      REGISTERS. BIT 7 HIGH PERMITTING
02DC 5C                 LR      S,A       OUTPUT OF SCAN DATA TO METR
02DD 2? 01 ??           PI      AVRG      CALL AVERAGING SUBROUTINE
02E0 4?                 LR      A,?       DATA TRANSFERRED TO
02E1 5?                 LR      H ? ?A    OUTPUT DATA REGISTER
02E2 4?         CONF    LR      A,?       CHECK THAT DATA READ WILL
02E3 25 1D              CI      H 1D      CAUSE A RETURN TO THE SEARCH MODE
02E5 8? 11              BC      REMN      BY FALLING OUTSIDE OF RIS
02E7 44                 LR      A,4       CLOSE AND TO TK2 OR STAY IN
02E8 25 E?              CI      H E?      TRACK (FALL THROUGH TO TK2)
02EA ?? ??              BNC     REMN
02EC 28 00 ??           PI      COMM2     DATA IN TRACK MODE THE CONE
02EF 6D         TK2     LISL    O 5       SET POINTER TO OUTPUT CONE
02F0 4?                 LR      A,?       SET BIT 5 HIGH INDICATING
02F1 22 20              OI      H 20      TRACK MODE OF OUTPUT CONE COUNTE
02F3 5?                 LR      S,A
02F4 29 01 ??   TK3     JMP     TRK1
02F7 6D         REMN    LISL    O 5       SETS BIT 5 LOW INDICATING
02F8 4?                 LR      A,?       SEARCH MODE
02F9 21 DF              NI      H DF
02FB 5?                 LR      S,A
02FC 90 F?              BR      TK3
```

PROGRAM LISTING

```
0263                     *ELEVATION ROUTINE
0264 02FE 0C        ELVN     PK                  ***ELEVATION ROUTINE, CLOCK TWO
0265 02FF 0C                 PK                  DRSK CLOCKS THEN CHECK FOR IDENT
0266 0300 40                 LR      A,0         WORD AND PARITY BITS
0267 0301 25 21              CI      H'21'
0268 0303 84 04              BZ      ATUD
0269 0305 29 03 0C           JMP     BREA
026A 0308 0C        ATUD     PK                  DRSK CLOCK 15
026B 0309 26 04              IN      H'04'       READ PILOTS CHOOSEN SEL G S
026C 030B 14                 SR      4           ANGLE   SHIFT INTO POSITION
026D 030C 13                 SL      1
026E 030D 24 DF              AI      H'DF'       THIS TRANSLATES ANGLE FOR INTER-
026F 030F 58                 LR      8,A         NALL TIMER
0270 0310 0C                 PK
0271 0311 0C                 PK                  DRSK CLOCK 17
0272 0312 48                 LR      A,8         CHECK THAT PILOT CHOOSE SDEG G
0273 0313 25 E7              CI      H'E7'       INDICATED BY  S DEG  INPUT
0274 0315 94 04              BNZ     LT8         (JUST THREE BITS ARE USED TO
0275 0317 20 FF              LI      H'FF'       INDICATE MAJOR DEGREES)
0276 0319 58                 LR      8,A         STORE 8 DEG
0277 031A 0C        LT8      PK                  DRSK CLOCK 18
0278 031B 20 37              LI      H'37'       TURN ON CCD RESET
0279 031D B0                 OUTS    H'00'
027A 031E 0C                 PK                  DRSK CLOCK 19
027B 031F 40                 LR      A,0         READ GRND FACILITY MIN G S
027C 0320 21 1F              NI      H'1F'       ANGLE (AN ANGLE OF 0 INDIC
027D 0322 84 05              BZ      COMP        8 DEGREES MIN G S
027E 0324 24 DF              AI      H'DF'       TRANSLATE MIN ANGLE FOR
027F 0326 90 06              BR      CALL        COMPARISON TO PILOTS
0280 0328 20 FF     COMP     LI      H'FF'       TRANSLATE  0  INPUT INTO 8 DEG
0281 032A 2B                 NOP                 NOPS EQUALIZE BRANCH TIMES
0282 032B 2B                 NOP
0283 032C 2B                 NOP
0284 032D 59        CALL     LR      9,A         STORE G S AND ALSO COMPARE TO
0285 032E 18                 COM                 PILOT S CHOOSEN ANGLE IF IT S
0286 032F 1F                 INC                 IS GREATER OR EQUAL TO MIN TURN
0287 0330 C8                 AS      8           WARNING LIGHT OFF, IF LESS THAN
0288 0331 82 05              BC      LTOF        MIN TURN WARNING LIGHT ON
0289 0333 20 FF     WARN     LI      H'FF'       TURNS WARNING LIGHT ON
028A 0335 90 06              BR      LTON
028B 0337 48        LTOF     LR      A,8         PILOTS ANGLE GREATER OR EQUAL TO
028C 0338 59                 LR      9,A         MINIMUM; PLACE PILOTS DATA IN TH
028D 0339 2B                 NOP                 REGISTER (NOP EQUALIZES BRANCH T
028E 033A 20 00              LI      H'00'       TURNS WARNING LIGHT ON
028F 033C 27 05     LTON     OUT     H'05'
0290 033E 20 04              LI      H'04'       READ OUTPUT STATUS OF MORSE
0291 0340 57                 LR      7,A         CODE, SO MUX OUT FOR LIGHT WON T
0292 0341 1F                 INC                 CHANGE STATUS (INC CHANGES MUX T
0293 0342 27 04              OUT     H'04'       TO LIGHT INPUT
0294 0344 47                 LR      A,7         RESTORE MUX STATUS OUT
0295 0345 27 04              OUT     H'04'
0296 0347 20 1F              LI      H'1F'       RESET DATA COUNTERS AND TURN CCD
0297 0349 B0                 OUTS    H'00'       RESET OFF
0298 034A 67                 LISU    O'7'        POINT TO ELEVATION UPDATE CONF
0299 034B 6D                 LISL    O'5'        REGISTER
029A 034C 4C                 LR      A,S         CHECK SEARCH TRACK BIT (5) FOR M
029B 034D 21 20              NI      H'20'       0 IS TRACK 1 IS SEARCH
029C 034F 84 04              BZ      SCM
029D 0351 29 07 DE           JMP     TMOD
029E                     *ELEVATION SEARCH MODE
029F 0354 20 C1     SCM      LI      H'C1'       *** ELEVATION SEARCH MODE, THIS
02A0 0356 1F        INC1     INC                 COUNTER TIMES THE DELAY TO START
02A1 0357 94 FE              BNZ     INC1        OF ENABLE OUTPUT
02A2 0359 20 1F              LI      H'1F'       RESET ALL DATA COUNTERS
02A3 035B B0                 OUTS    H'00'
02A4 035C 20 29              LI      H'29'       RESET TURNED OFF ENABLE 300KHZ
02A5 035E B0                 OUTS    H'00'
02A6 035F 20 50              LI      H'50'       DURATION TIMER
02A7 0361 1F        INC2     INC
02A8 0362 94 FE              BNZ     INC2
02A9 0364 70                 CLR                 CLEAR DATA PORT
02AA 0365 B1                 OUTS    H'01'
02AB 0366 A1                 IN      H'01'       READ DOWN DATA
02AC 0367 54                 LR      4,A         STORE DOWN DATA
02AD 0368 28 00 60           PI      STROBE      STROBE FW THROUGH LATCH
02AE 036B 70                 CLR                 CLEAR DATA PORT
02AF 036C B1                 OUTS    H'01'
02B0 036D A1                 IN      H'01'       READ DOWN FW
02B1 036E 55                 LR      5,A         STORE DOWN FW
02B2 036F 28 00 54           PI      RESET       RESET COUNTERS AND TIME MIDSCAN
02B3 0372 20 2B              LI      H'2B'       UP SCAN ENABLE
02B4 0374 B0                 OUTS    H'00'
02B5 0375 20 50              LI      H'50'       UP SCAN DURATION TIMER
02B6 0377 1F        INC3     INC
02B7 0378 94 FE              BNZ     INC3
02B8 037A 70                 CLR                 CLEAR DATA PORT
02B9 037B B1                 OUTS    H'01'
02BA 037C A1                 IN      H'01'       READ THE UP SCAN DATA
02BB 037D 56                 LR      6,A         STORE UP SCAN DATA
02BC 037E 28 00 60           PI      STROBE      STROBE FW       INTO LATCH
02BD 0381 70                 CLR                 CLEAR DATA PORT
02BE 0382 B1                 OUTS    H'01'
02BF 0383 A1                 IN      H'01'       READ UP SCAN FW
02C0 0384 57                 LR      7,A         STORE FW
02C1 0385 28 00 54           PI      RESET       RESET ALL COUNTERS, **DATA WORDS
```

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PROGRAM LISTING

```
                        *LOOK FOR DATA WORD ONE BEFOR CON T
0388 20 15              LI      H 15    CK FOR DAT WRD 1 BEFOR AN.
038A 51                 LR      1,A     EL CALCULATION  SEARCH ONLY 15 D
038B 0C        CPK      PK              CLOCKS (DPSK CK TIMER)
038C 25 54              CI      H 54    LOOK FOR ID WORD PARITY & LAST
038E 84 06              BZ      LID     2 BARKER BITS
0390 31                 DS      1
0391 94 F9              BNZ     CPK
0393 90 15              BR      ELEO
0395 20 0A     LID      LI      H 0A    DPSK CLOCKS TO APPEARENCE OF
0397 51                 LR      1,A     CATAGORY GRND FACILITY BITS
0398 0C        CPK1     PK
0399 31                 DS      1
039A 94 FD              BNZ     CPK1
039C 64                 LISU    D 4     POINT TO DATA WORD CONF
039D 6B                 LISL    D 3     COUNTER
039E 21 03              NI      H 03    MASK CAT BITS
03A0 84 06              BZ      DFCO    IF BOTH ARE ZERO CLEAR DATA WORD
03A2 20 20              LI      H 20    IF EITHER OR BOTH ARE HIGH INC
03A4 5C                 LR      S,A     CONF COUNTER WITH CONSTANT
03A5 90 03              BR      ELEO
03A7 70        DFCO     CLR             CLEAR DATA CONF
03A8 5C                 LR      S,A
                        *RETURN TO EL SEARCH MODE CAL
03A9 67        ELEO     LISU    D 7     BRING POINTER BACK TO EL SECTION
03AA 28 00 C1           PI      ELSPW   PW & COLD CHECK IF PASSESDD
03AD 28 00 6F           PI      CONEL   INC CONF COUNNTERS
03B0 20 AD              LI      H AD    MIN VAL TO ENTER TRACK MODE
03B2 56                 LR      6,A     TO THIS VALUE A CONSTANT IS ADDE
03B3 49                 LR      A,9     THAT IS PROPORTIONAL TO THE SEL
03B4 18                 COM             ANGLE
03B5 1F                 INC
03B6 59                 LR      9,A
03B7 20 02              LI      H 02    02 IS ADDED TO AD  BY A LOOP
03B9 57                 LR      7,A     THAT DEPENDS ON G S READING
03BA 70                 CLR             AT THE COUNTER
03BB C7        INCRE    AS      7
03BC 39                 DS      9
03BD 94 FD              BNZ     INCRE
03BF C6                 AS      6       ADD VARIABLE SUM TO THE BASE CON
03C0 56                 LR      6,A     THIS VALUE IS MIN TO ENTER THE T
03C1 18                 COM             MODE, SUBT TOTAL VALUE FROM DATA
03C2 1F                 INC             IF LESS GO TO FLY DOWN MODE
03C3 C4                 AS      4
03C4 6E                 LISL    D 6     POINT TO OUTPUT DATA REG
03C5 92 0C              BNC     DOWN
03C7 46                 LR      A,6     IF MORE THAN MIN VALUE
03C8 24 05              AI      H 05    ADD CONSTANT 05 TO OBTAIN
03CA 18                 COM             MAX VALUE , CHECK IF LESS THAN
03CB 1F                 INC             MAX VALUE IF SO GO TO TRACK MODE
03CC C4                 AS      4       OTHWISE KEEP IN SEARCH
03CD 82 0A              BC      UP      METER DIFF UP OR DWN AS REQUIRED
03CF 29 04 4D           JMP     CGMD
03D2 20 0C     DOWN     LI      H 0C    DEFLECT METER DOWN
03D4 5C                 LR      S,A     STORED FOR METER SERVICE
03D5 29 04 54           JMP     CGSH
03D8 20 0E     UP       LI      H 0E    FULL DIFFLECTION UP
03DA 5C                 LR      S,A     STORED FOR METER SERVICE
03DB 29 04 54           JMP     CGSH
                        *ELEVATION TRACK MODE ROUTINE
03DE 20 90     TMOD     LI      H 90    ***ELEVATION TRACK ROUTINE, THIS
03E0 1F        INC4     INC             COUNTER DELAYS THE START OF TRAC
03E1 94 FE              BNZ     INC4    GATES WHOSE START IS VARIABLE
03E3 49                 LR      A,9     PROPORTIONALLY WITH THE SEL G S A
03E4 2B        TWELVE   NOP             TWELVE MICRO SEC DELAY FROM
03E5 2B                 NOP             BY THE SEL G S ANGLE
03E6 1F                 INC
03E7 94 FC              BNZ     TWELVE
03E9 20 39              LI      H 39    ENABLE TRACK MODE DOWN SCAN GATE
03EB B0                 OUTS    H 00
03EC 20 E0              LI      H E0    DURATION OF GATE IN FRONT PORCH
03EE 1F        INC5     INC             ALLOWING PW WIDER THAN
03EF 94 FE              BNZ     INC5    GATE WINDOW TO BE HANDLED
03F1 20 3D              LI      H 3D    TURN GATE OFF ,,PORCH ALLOWS
03F3 B0                 OUTS    H 00    COUNTER TO REVOLVE TWICE ,
03F4 70                 CLR             CLEAR DATA PORT ,FIRST REV CON I
03F5 B1                 OUTS    H 001   SECOND REV CON IDERED POS,
03F6 A1                 INS     H 01    READ DATA
03F7 54                 LR      4,A     STORE DOWN SCAN DATA
03F8 20 DD              LI      H DD    DELAY PR AND CCD RESET SO NOT
03FA 1F        INC6     INC             CHOP PW READING
03FB 94 FE              BNZ     INC6
03FD 28 00 80           PI      STRORE  STORE PW THRU LATCH RESET CCD
0400 70                 CLR             CLEAR THE DATA PORT
0401 B1                 OUTS    H 01
0402 A1                 INS     H 01    READ DOWN SCAN PW
0403 55                 LR      5,A     STORE DOWN SCAN PW
0404 20 1F              LI      H 1F    RESET THE DATA COUNTERS
0406 27 00              OUT     H 00
0408 20 FC              LI      H FC    MIDSCAN DURATION TIMER WHICH
040A 1F        CL11     INC             IS MODIFIED BY A COUNTER
040B 94 FE              BNZ     CL11    THAT IS PROGRAMABLE BY THE
040D 49                 LR      A,9     SEL G S, THE SEL G S ANGLE HAS
040E 24 21              AI      H 21    21 ADDED TO IT TO COMPLEMENT
0410 13                 SL      1       IT 9 DEG. MULT BY 2 BECAUSE THE
0411 59                 LR      9,A     TO SCAN GATE CHANGES POSITION
0412 30        TWLV     DS      0       THE PRO MUST CHANGE DOUBLE
0413 39                 DS      9       THE 9 DEGREE COMP
0414 94 FD              BNZ     TWLV    DS 0,DS 9, ARE 12 MIC SEC
0416 20 3B              LI      H 3B    DELAY LOOP  (ENABLE GATE)
```

PROGRAM LISTING

```
0326 0418 B0                 OUTS   H 00
0327 0419 20 E0      CL12    LI     H E0     DURATION OF TRACK UP SCAN GATE
0328 041B 1F                 INC
0329 041C 94 FC              BNZ    CL12
032A 041E 20 3F              LI     H 3F     TURN GATE ENABLE OFF
032B 0420 B0                 OUTS   H 00
032C 0421 70                 CLR             CLEAR INPUT DATA PORTT
032D 0422 B1                 OUTS   H 01
032E 0423 A1                 INS    H 01     READ UP SCAN DATA
032F 0424 56                 LR     6,A      STORE UP SCAN DATA
0330 0425 20 EE              LI     H EE     DELAYS PE & CCD RESET SO TO NOT
0331 0427 1F         CL13    INC             CHOP PW
0332 0428 94 FE              BNZ    CL13
0333 042A 28 00 60           PI     STROBE   STROBE PW THROUGH LATCH
0334 042D A1                 INS    H 01     READ PW
0335 042E 57                 LR     7,A      STORE UP SCAN PW
0336 042F 28 00 54           PI     RESET    RESET ALL DATA COUNTERS
0337 0432 28 00 CD           PI     FLTPW    CHECK PW & COLOCATION
0338 0435 44                 LR     A,4      CHECK THAT DATA ISN T RANGE FOR
0339 0436 25 1D              CI     H 1D     FOR A RETURN TO SEARCH MODE
033A 0438 92 1B              BC     CSCH
033B 043A 28 01 03           PI     AVRG     TRACK MODE CALL AVERAGING ROUTIN
033C 043D 2A 03 30           DCI    H 0330         **SELECTABLE 0 : ANGLE
033D 0440 49                 LR     A,9      COMPENSATION PROG BY SEL ANGLE
033E 0441 12                 SR     1        1 4 DEG INC IGNORED SHIFTED OUT
033F 0442 8E                 ADC             CONTENTS CONTAINED IN MEMORY
0340 0443 53                 LR     3,A      IS CHOSEN ACORDING TO S
0341 0444 83                 AM              ANGLE AND ADDED TO DATA BEFOR
0342 0445 5B                 LR     H B,A    STORING FOR METER SERVICE
0343 0446 28 00 8E           PI     CONFL    PASSED COLO IN CONF
0344 0449 6B                 LISL   3 6      POINT TO OUTPUT DATA REG
0345 044A 20 03              LI     H 03     SET DATA OUTPUT BIT HIGH
0346 044C 5C                 LR     S,A
0347 044D 6A         CGND    LISL   0 5      POINT TO OUTPUT CONF REG
0348 044E 4C                 LR     A,S
0349 044F 22 20              OI     H 20     SET S T BIT HIGH (TRACK MODE)
034A 0451 5C                 LR     S,A
034B 0452 90 06              BR     CALNT
034C 0454 6A         CSCH    LISL   0 5      POINT TO OUTPUT CONF REG
034D 0455 4C                 LR     A,S
034E 0456 21 DF              NI     H DF     SET S T BIT LOW (SEARCH MODE)
034F 0458 5C                 LR     S,A
0350 0459 29 01 46   CALNT   JMP    BKKS
0351                 .
0352                 .
0353                 .
0354                         END
00

ADDM 0126  ALDC 0127  ACFW 00AB  ATFW 00B7  ATOD [illegible]
AONE 01[illegible]  ACRR 01[illegible]  ATIN [illegible]1D
                                        BIFA 019D  BKK1 01[illegible]D  BKK2 01[illegible]  BKK3 012[illegible]  BKKS
0146
CALL [illegible]  CALN 0459  CERA [illegible]  CENT 01FS  CF1 [illegible]
CGND 044D  CSCH 0454  CL11 [illegible]  CL12 0419  CL13 0427
CLD2 [illegible]  CLD3 [illegible]  CLD4 [illegible]  CLD5 [illegible]  CLD6 [illegible]
CLD7 [illegible]  CLD8 [illegible]  CLD9 [illegible]  CLDA [illegible]  CLR [illegible]
[illegible]  COLD [illegible]  COLC 00E1  CONF [illegible]  CONH [illegible]
CONS [illegible]  CONF [illegible]  CR [illegible]  CR1 [illegible]  CN [illegible]
DIRN 014F  DSRN 01EF  DOUC [illegible]  DOUT [illegible]  DAT1 [illegible]
DAT2 [illegible]  DATB 01FS  DEC [illegible]  DECT 01EF  DIVD [illegible]
DMS [illegible]  DOWN [illegible]  DST [illegible]  DSRN [illegible]  FLED [illegible]
EL F [illegible]  FLTP [illegible]  FL [illegible]  FLVH [illegible]  ID [illegible]
INCH [illegible]  INC1 [illegible]  INC2 [illegible]  INC3 [illegible]  INC4 [illegible]
INC5 [illegible]  INC6 [illegible]  INCF [illegible]  INTL [illegible]  LEFT [illegible]
LET [illegible]  LID [illegible]  LD [illegible]  LOOP [illegible]  LT [illegible]
LTOF [illegible]  LTON [illegible]  MOT [illegible]  MRK [illegible]  NET [illegible]
NSN [illegible]  OFLO [illegible]  OFST [illegible]  ONE [illegible]  PLUS [illegible]
PRO [illegible]  PW [illegible]  PWEN 0121  PENM [illegible]  RESE [illegible]
SGT 01DD  RIGH [illegible]  SCH [illegible]  SCHM [illegible]  SERV [illegible]
SET [illegible]  SET2 01F1  SETS [illegible]  STFL [illegible]  STRB [illegible]
TK [illegible]  TK [illegible]  TMOD [illegible]  TRAC [illegible]  TRCK [illegible]
TRO 0101  TT [illegible]  TWEL [illegible]  TWLV 0412  UNFG [illegible]
UP [illegible]  WASH [illegible]
.
?00
```

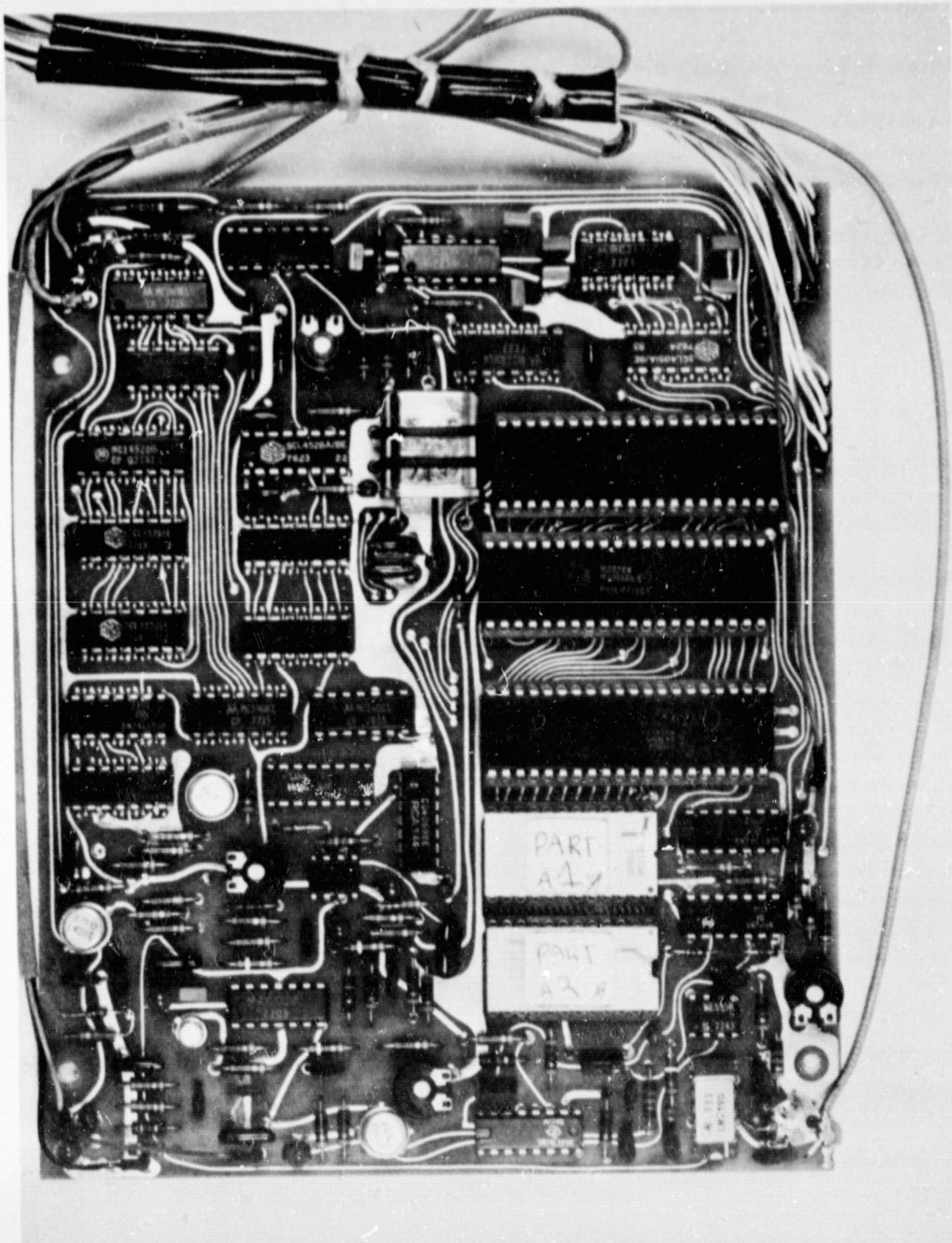


FIGURE 56. PROCESSOR TOP VIEW

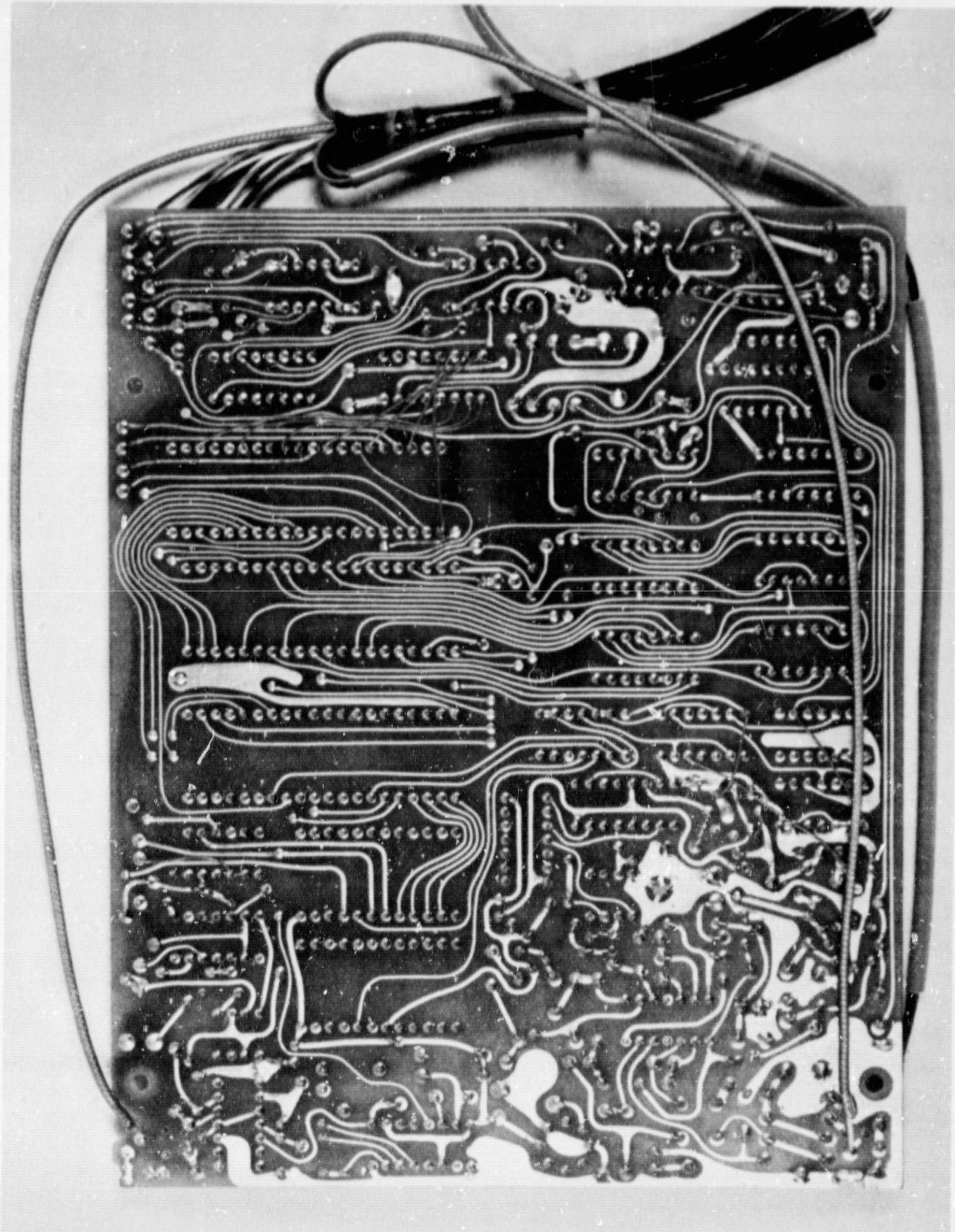


FIGURE 57. PROCESSOR BOTTOM VIEW

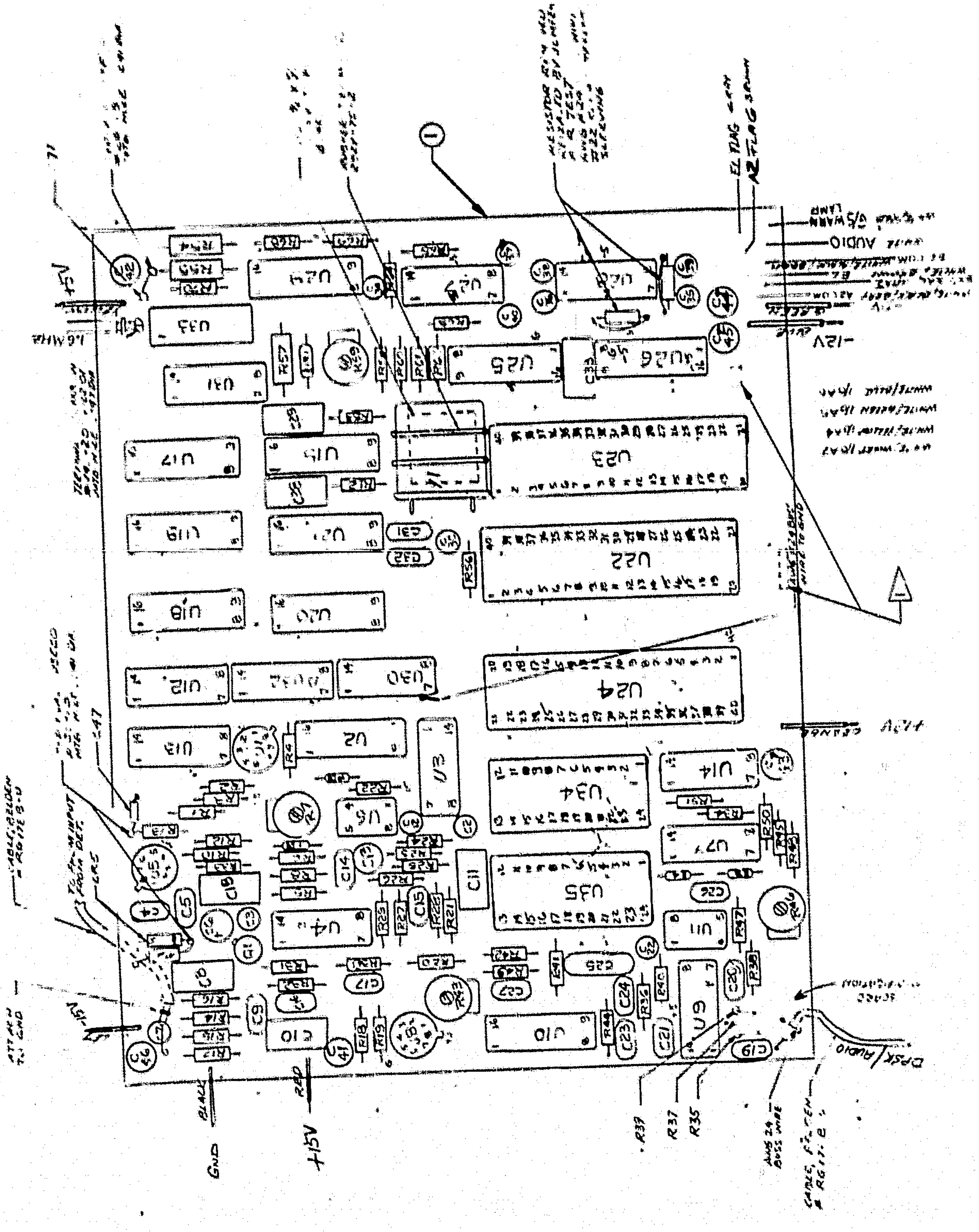


FIGURE 58. BOARD ASSEMBLY, PROCESSOR

Integrated MLS Receiver

The following assemblies make up the MLS receiver:

1. RF Head
2. IF/Detectors
3. Synthesizer
4. Processor
5. Power Supply
6. Mechanical

The power supply and mechanical assemblies are described briefly within this portion, but are not to be considered critical. It is expected that any manufacturer contemplating the production of this equipment would want to utilize his existing designs of power supply and mechanical package. In fact, the package and power supply of the MLS receiver described herein are minor modifications of existing NARCO product line assemblies.

POWER SUPPLY

The power supply for the Low Cost MLS Receiver is not considered critical, since several very low cost circuits that will meet the requirements are available and have already been optimized for performance/cost. Accordingly, since this assembly is already low cost, it was not efficient to study techniques extensively to reduce the cost further. The highly similar NARCO DME-190 supply was used as the cost baseline.

A block diagram of the power supply subassembly is shown in Figure 59. The design is similar to that utilized in the DME-190 distance measuring equipment manufactured by NARCO and is fully capable of meeting the input power characteristics of RTCA document DO-160. The nominally 11 VDC to 33 VDC power from the aircraft is initially filtered for transient protection and then applied to a switching regulator composed of transistors Q1 and Q2 and integrated circuit U1. The output of this regulator is +7 VDC. This output is used by receiver logic (after local regulation) and is also routed to the DC to AC converter composed of Q3, Q4, and T1. The resulting AC outputs are rectified and filtered to supply ± 15 VDC for use by the receiver analog circuits. The operating frequency of the DC to DC converter is chosen so as to not be fundamentally or harmonically related to the 15 kHz system data rate. The overall efficiency of the supply is 80% minimum.

The schematic diagram for the power supply is shown in Figure 60. The parts list is presented in the Appendix of this report.

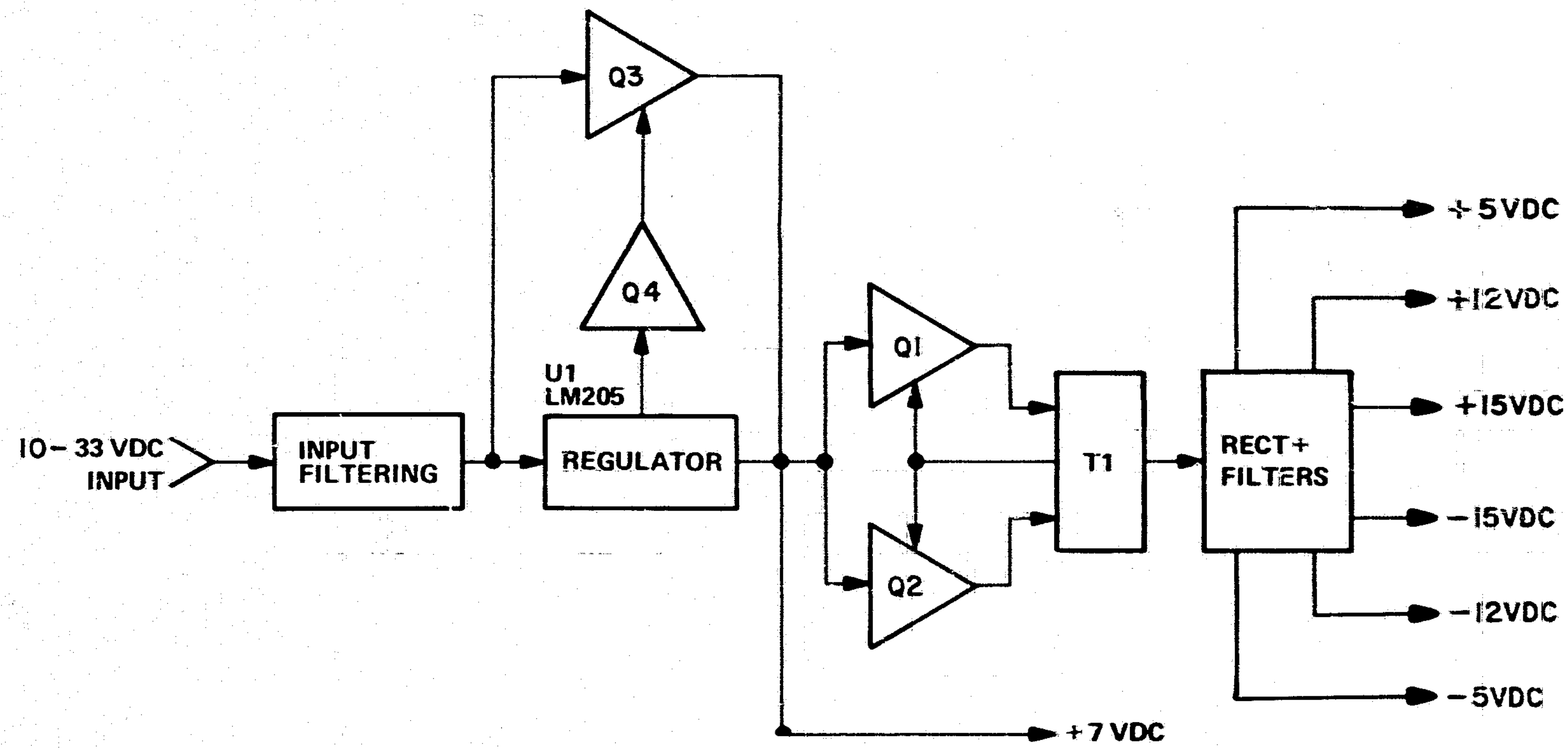
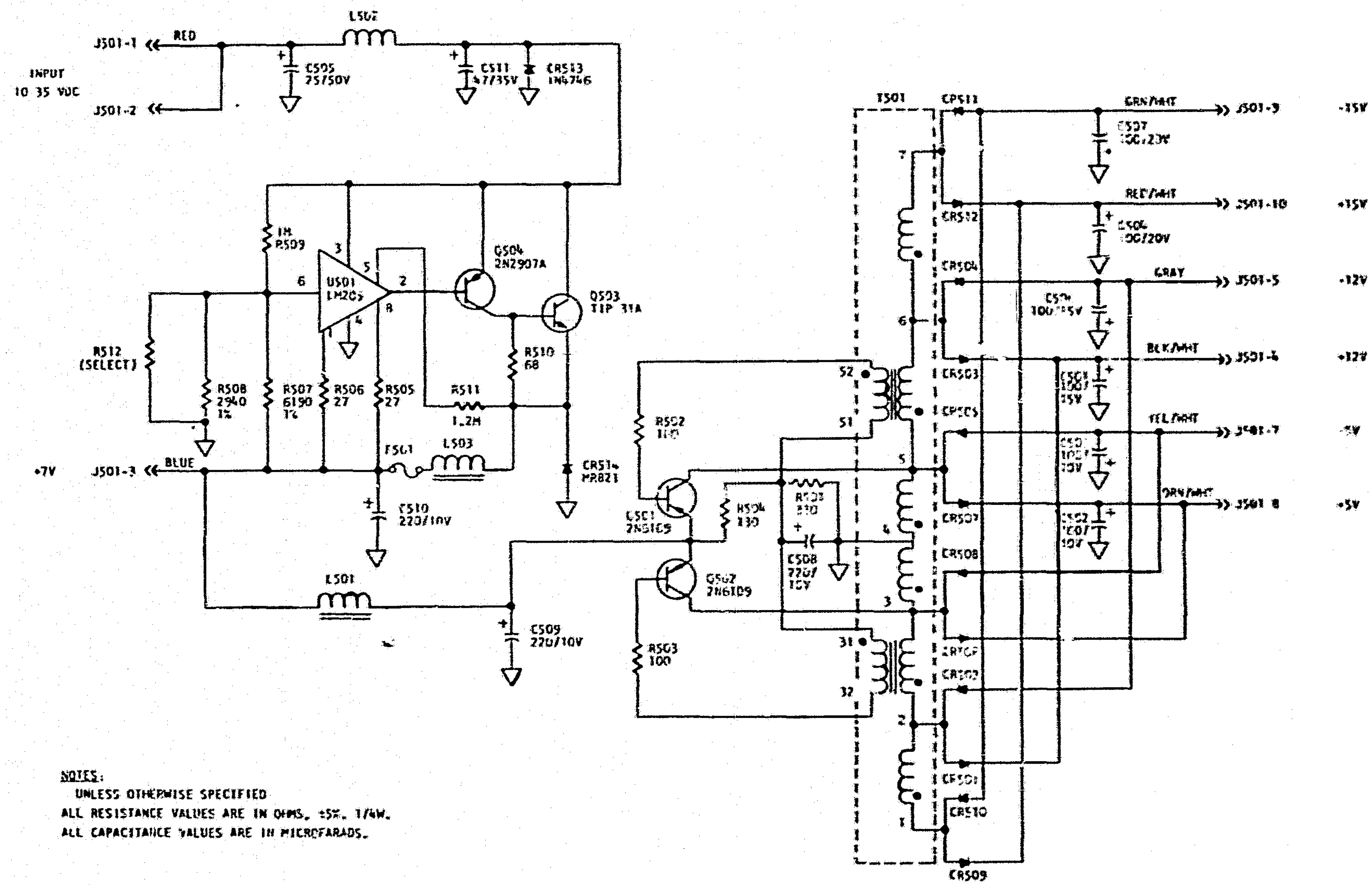


FIGURE 59. POWER SUPPLY BLOCK DIAGRAM



NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W.
ALL CAPACITANCE VALUES ARE IN MICROFARADS.

FIGURE 60. POWER SUPPLY SCHEMATIC

MECHANICAL SUBASSEMBLY

The packaging for the Low Cost MLS Receiver is highly similar to the NARCO DME 190. This unit has already been optimized for cost/performance. An extensive additional effort for further cost reduction was not considered necessary.

The panel mounted MLS receiver is packaged using the proven features of the productized NARCO DME-190. The remote RF head is packaged separately with an integral antenna.

The MLS prototype receiver panel mounted unit is constructed as a unit divided into four major mechanical subassemblies. The Frontispiece Trim Panel Assembly, the Mainframe, the Power Supply (integrated into Mainframe), and the Hinged Panel.

The trim panel assembly consists of a die-cast front panel incorporating all the features required to hold, operate, and display the dials, knobs, and indicators. In addition, the back face of the panel provides the mounting provision for the integrated PC board and wafer switches. Mounting provisions are made to mount the panel integrally to the receiver. Figures 61 and 62 show the panel mounted unit front and rear views.

The mainframe assembly is composed of the side panel stampings and rear extrusions to form the basic structural envelope of the receiver. Each structural member is designed to be multifunctional. The rear panel extrusion, as an example, contains the heat sink fins to provide convective cooling to the ambient air (ram air is not required). In addition, it provides a firm mounting plane to assemble the center section power supply.

The processor assembly is mounted on one hinged panel within the mainframe. Since this assembly is predominantly digital, with no RF circuitry whatsoever, no alignment is expected and no shielding is necessary. A photograph of the processor panel in the swing-out position is shown in Figure 63.

A second hinged panel is provided which contains the IF/Detector and Synthesizer assemblies. A photograph of the swing-out panel containing the IF/Detector and Synthesizer assemblies is shown in Figure 64.

The four major mechanical subassemblies, when assembled, form a rigid, unified structure, which when combined with the aircraft mounting frame, is capable of meeting all dynamic environmental test requirements.

Additional packaging design objectives will be ease of maintenance and accessibility. Subassemblies are designed for low cost assembly time while still allowing for in-process inspection and on-line repair.

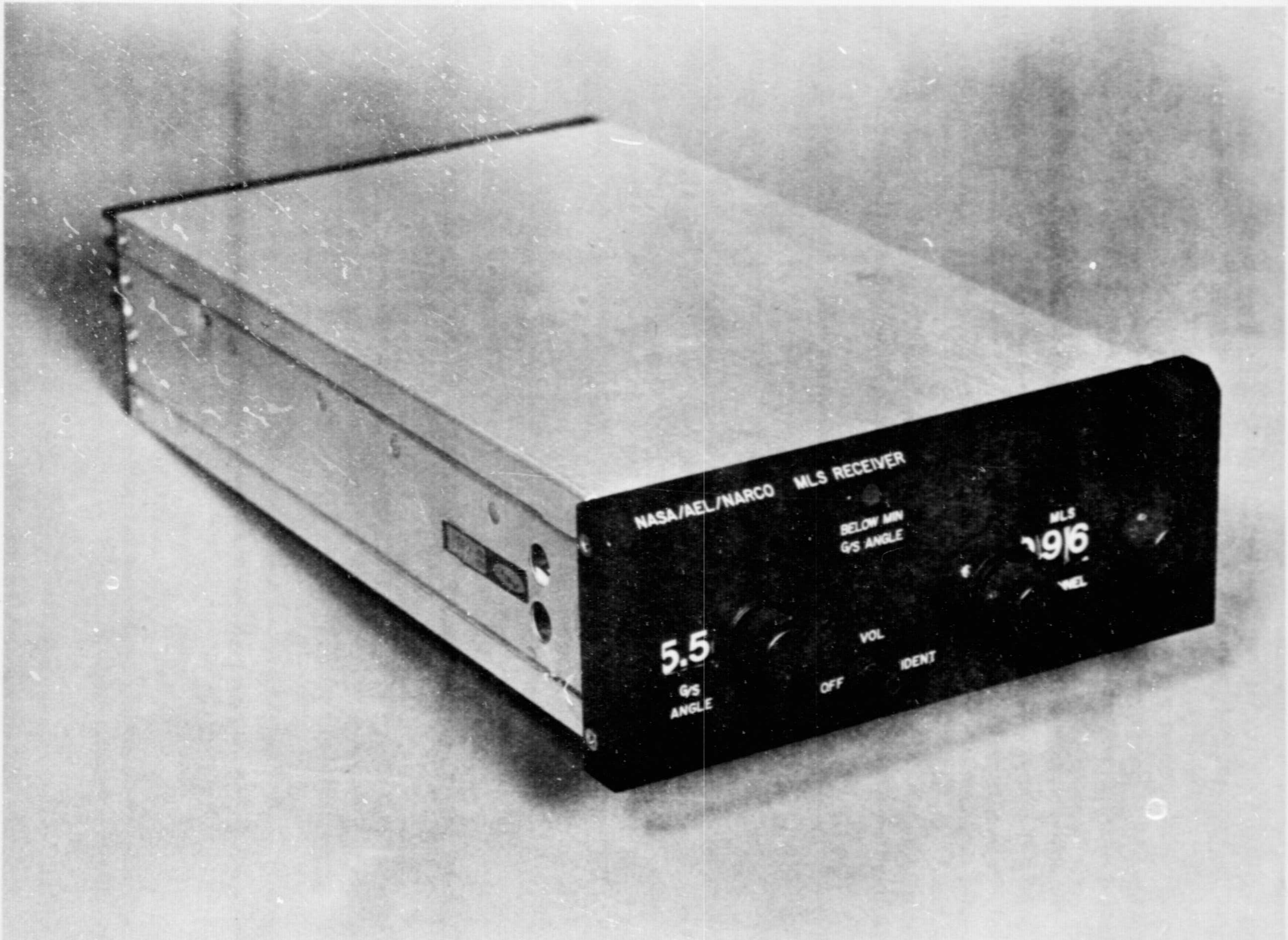


FIGURE 61. FRONT VIEW, PANEL MOUNTED UNIT

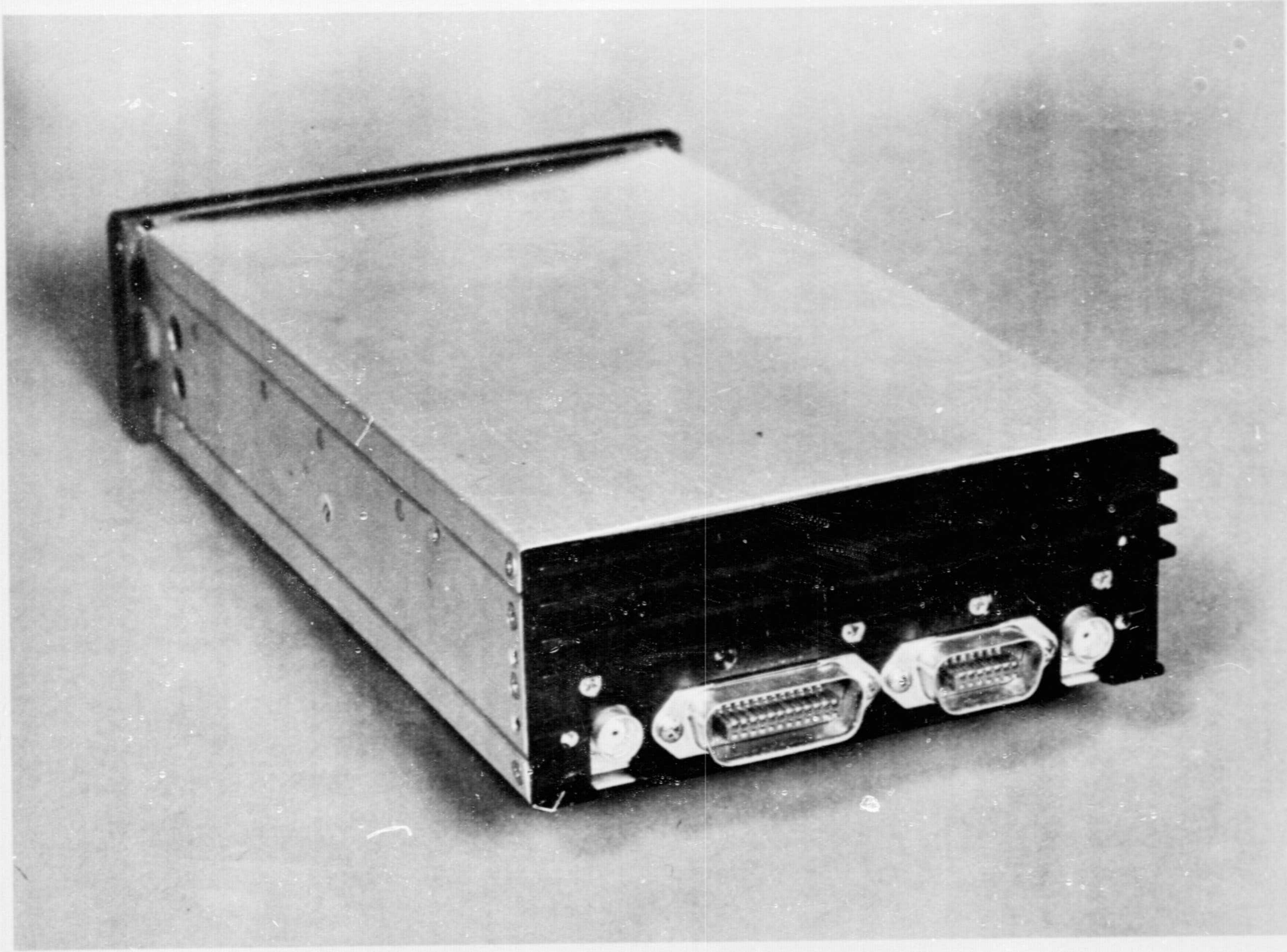


FIGURE 62. REAR VIEW PANEL MOUNTED UNIT

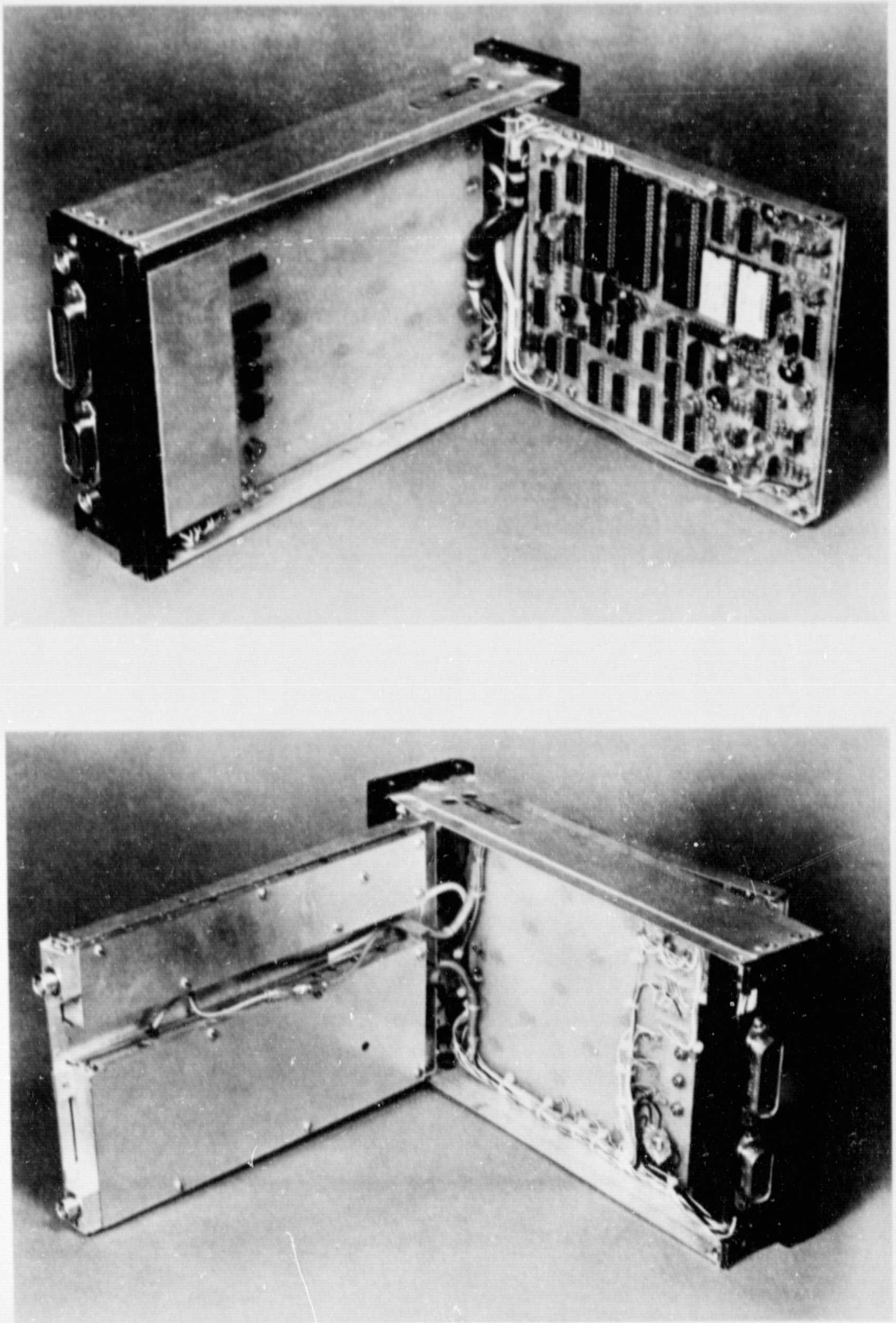


FIGURE 63. PROCESSOR PANEL, IF/DETECTORS AND SYNTHESIZER PANEL

Mechanical Mounting

The mechanically packaged candidate system consists of a box containing the electronic components and control elements, as shown in Figure 61. A tray is mounted in the airplane instrument panel in the standard manner, which conforms in size to the industry standards. The receiver box is constructed to slide into this tray and mate with connectors contained within the tray. A locking mechanism secures the box in the tray. The front of the box mounts a trim panel, an on/off switch, an ident volume control, and selector switch and indicator for selecting a particular glideslope angle. From the tray, DC power and control cable connection are provided to external loads such as the power source, and deviation indicator, and other outputs such as the autopilot. Two coaxial cables are provided to a hermetically sealed RF head which contains the functions of RF preselector, first mixer, first IF amplifier, and first LO multiplier. This RF head will be mounted directly on the airplane skin since it contains an integrated antenna.

In order to allow automatic component lead insertion techniques onto the printed wiring cards, the low cost MLS receiver panel mounted unit utilizes a chassis of 10 inches long and 160 cubic inches volume.

This length is desirable to maintain a consistent avionics equipment depth in the stack, since standard avionics panel mounted units are 10 inches deep or 160 cubic inches in volume. A shorter unit could be detrimental since the rear heat sink would not be properly exposed to the air space available.

An exploded view of the MLS Receiver is shown in Figure 64, followed by the mechanical parts list.

ELECTRICAL INTERCONNECTIONS

The various assemblies of the MLS receiver are interwired by cabling and harness, to produce the final panel mounted unit assembly. Figure 65 shows the interconnection schematic. Note that the digital and analog DPSK and video outputs of J2 are not required for general aviation equipment but were included on the prototype receivers for test purposes. A pictorial wiring diagram is shown in Figure 66.

Antenna Mounting

The RF Head must be mounted on a relatively free and clear surface, without obstruction in the forward direction. An ideal location is atop the cabin for a single engine plane, as shown in Figure 67. For twin engine planes, the ideal area is the top of the cabin nose.

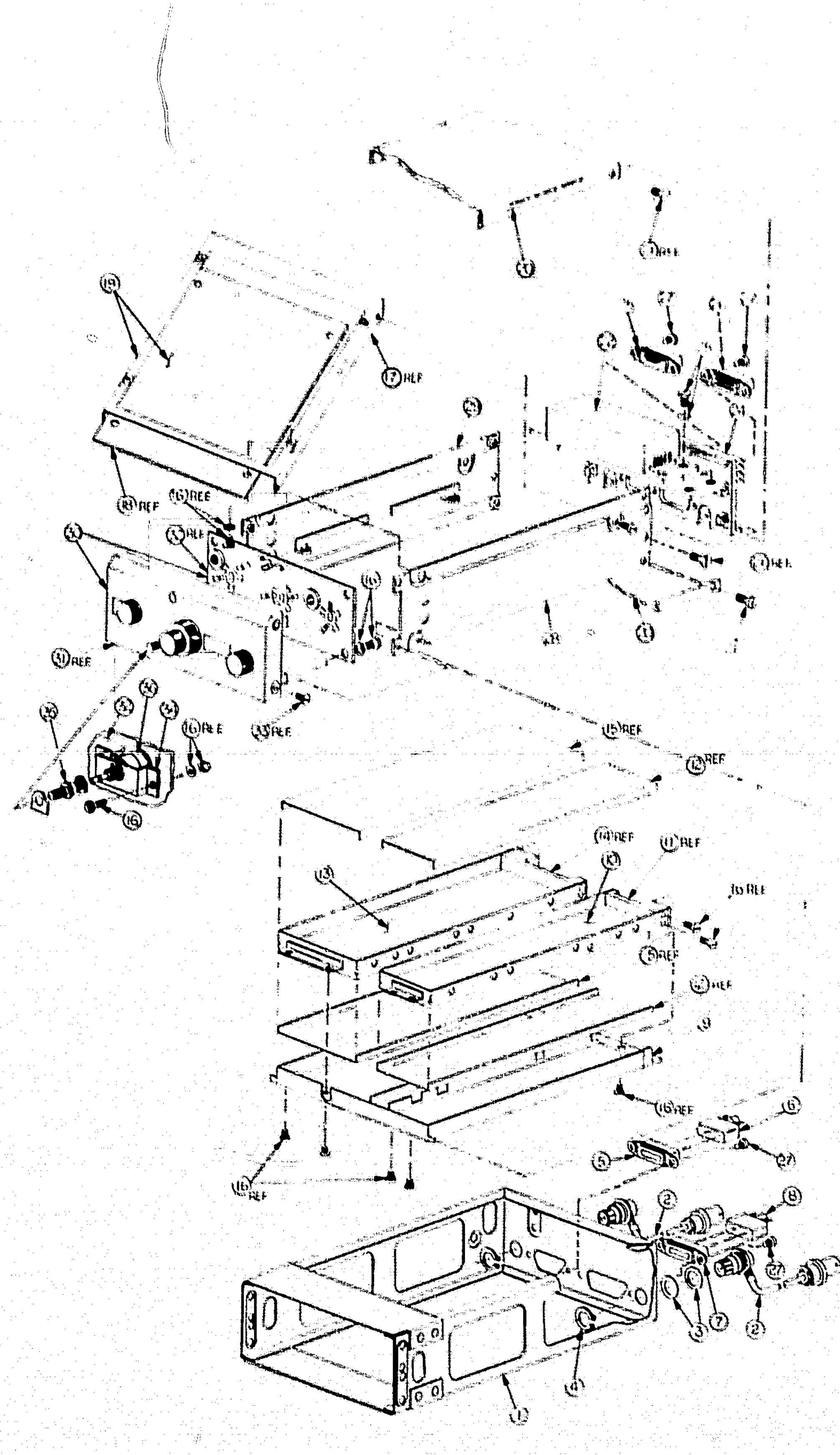


FIGURE 64. MLS RECEIVER EXPLODED VIEW DRAWING

MECHANICAL PARTS LIST

FIG. & ITEM NO.	PART NUMBER	DESCRIPTION
-1	53239-0101	TRAY ASSEMBLY
-2	90701-0101	ANTENNA CABLE ASSEMBLY
-3	81307-0112	WASHER, FLAT
-4	81192-0024	RING, RETAINING
-5	41286-0002	CONNECTOR, Receptacle, 14 Pin
-6	41385-0001	CONNECTOR HOOD (14 Pin)
-7	41286-0004	CONNECTOR, Receptacle, 24 Pin
-8	41385-0002	CONNECTOR HOOD (24 Pin)
-9	53236-0001	BOTTOM BRACKET ASSEMBLY
-10	01340-0101	ASSEMBLY, IF Detector M.L.S. Receiver Board
-11	53230-0001	BLOCK BNC ADAPTER
-12	53241-0001	COVERS - Top & Bottom Receiver
-13	01341-0101	ASSEMBLY, Synthesizer M.L.S. Receiver Board
-14	53229-0001	BLOCK BNC ADAPTER
-15	53242-0002	COVERS - Top & Bottom Synthesizer
-16	82958-0002	SCREW, Mach, Pan Hd, Slotted No. 4
	82802-0003	WASHER, Lock, No. 4 (Used where noted)
	82900-0004	NUT, Hex, No. 4 (Used where noted)
-17	53237-0001	TOP FRAME BRACKET ASSEMBLY
-18	53248-0101	PROCESSOR P.C. BOARD
-19	01342-0101	TOP FRAME & PROCESSOR BOARD ASSEMBLY
-20	57726-0001	COVERS - Top & Bottom
-21	82819-0303	SCREW, Mach, Flat Hd, Slotted No. 4
-22	01289-0102	ASSEMBLY, Power Supply, M.L.S.
-23	82892-0003	SCREW, Mach, Pan Hd, Slotted, No. 4
	82802-0003	WASHER, Lock, No. 4

MECHANICAL PARTS LIST

FIG. & ITEM NO.	PART NUMBER	DESCRIPTION
-24	53226-0001	HEAT SINK REAR
-25	41286-0001	CONNECTOR PLUG, 14 Pin
-26	41286-0003	CONNECTOR PLUG, 24 Pin
-27	82826-0002	SCREW, Mach, Rd Hd, No. 3
	82807-0033	WASHER, Lock, No. 3
-28	53255-0001	SIDE PANEL (Left)
-29	53255-0002	SIDE PANEL (Right)
-30	01344-0101	ASSEMBLY, Trim Panel w/Switch Board
-31	53225-0001	TRIM PANEL
-32	01343-0101	ASSEMBLY, Switch Board
-33	82819-0304	SCREW, Mach, Flat Hd, Flat Black Slotted, No. 4
-34	53238-0001	BRACKET, Volume Control
-35	56250-0001	KNOB, Volume Control
-36	32070-0002	VARIABLE RESISTOR & SWITCH

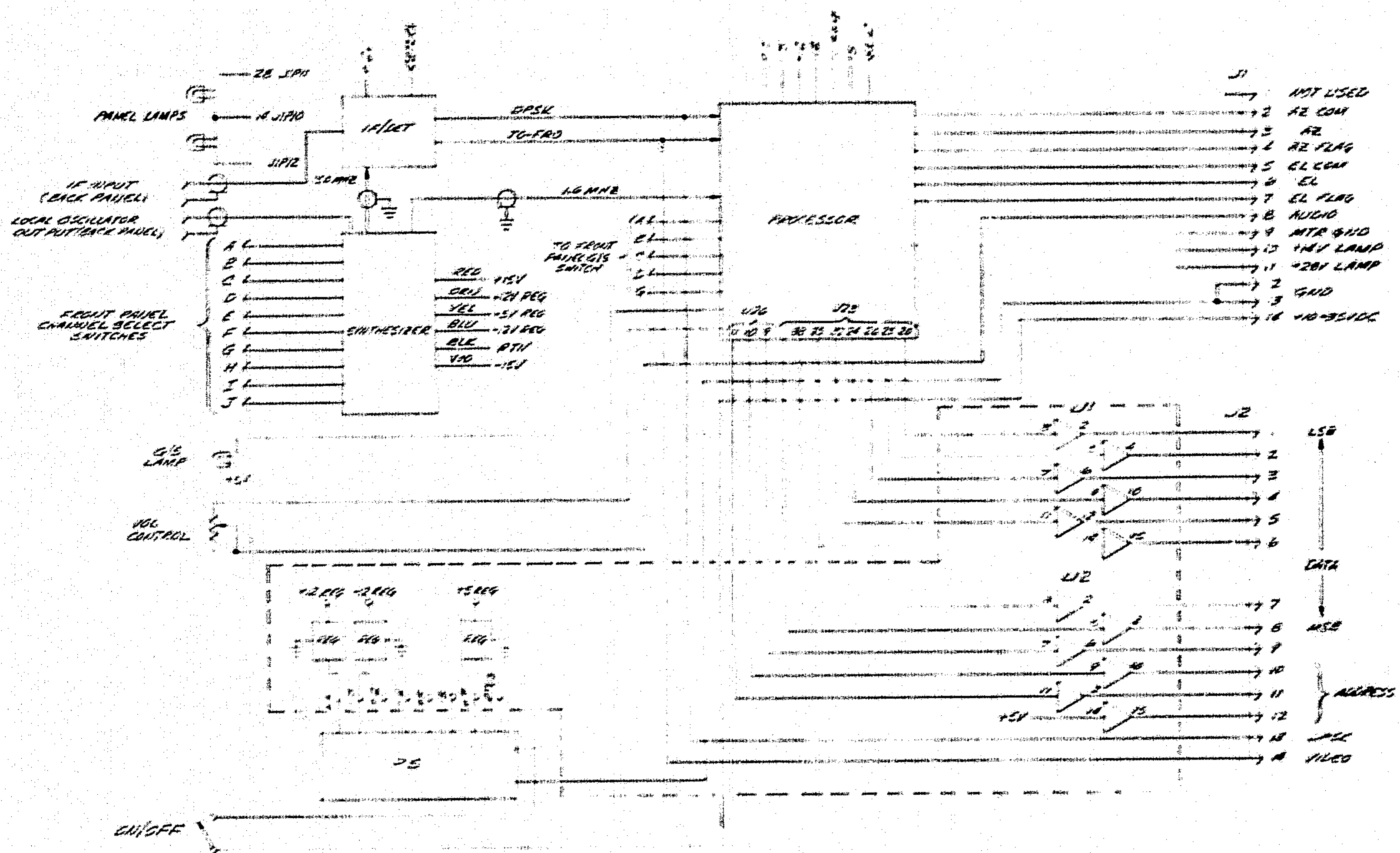


FIGURE 65. INTERCONNECTION DIAGRAM, MLS RECEIVER

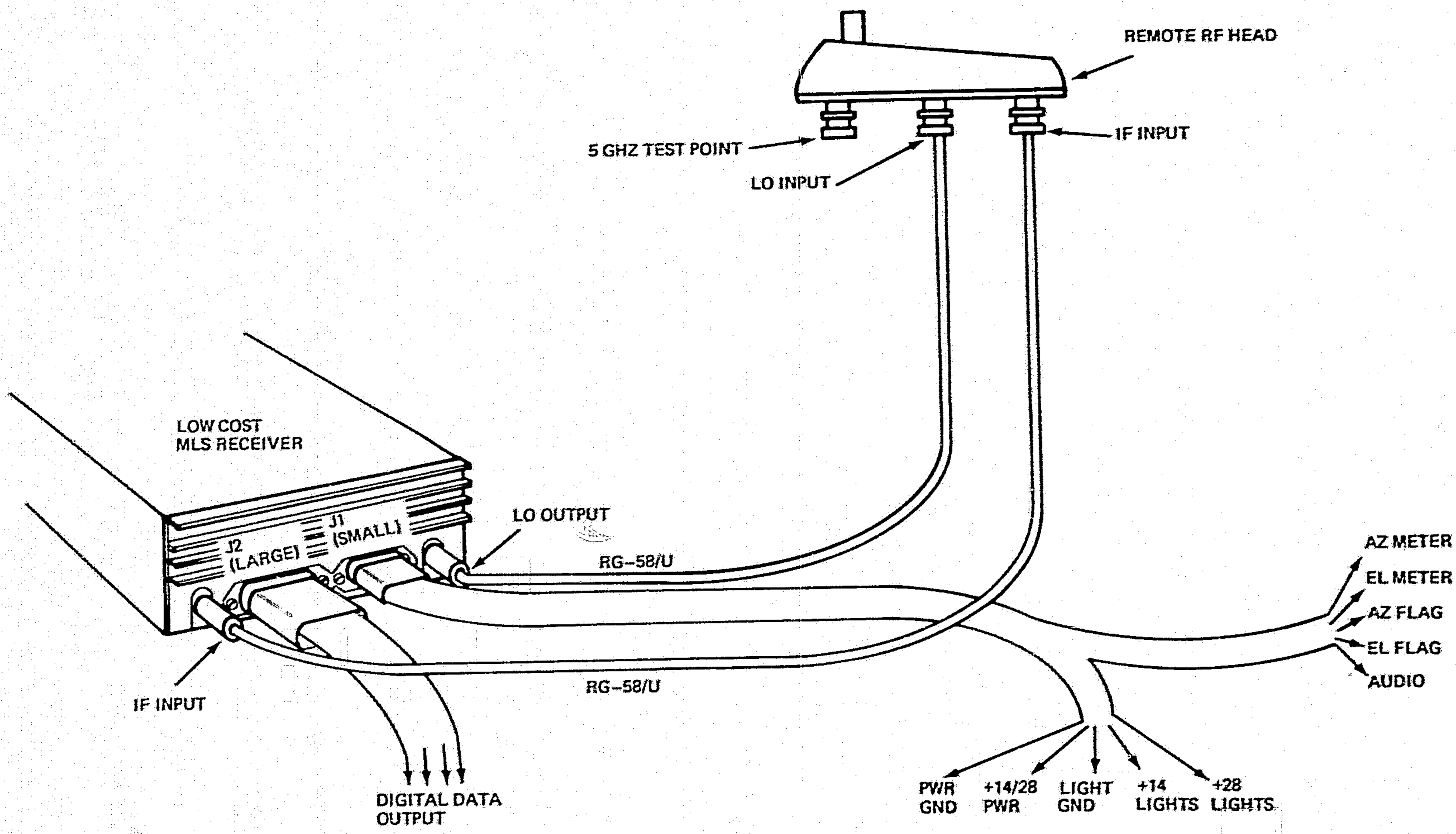


FIGURE 66. PICTORIAL WIRING DIAGRAM

FIGURE 67. LCMLS ANTENNA INSTALLATION

COMPATIBILITY WITH MLS GROUND SYSTEMS

The low cost MLS receiver was designed to receive and operate with ground signals meeting the format requirements of FAA-ER-700-08A dated 30 May 1975 and Ammendment #1 dated 22 August 1975.

It was found, however, that this specification did not firmly establish all parameters of the signal and that minor but significant differences between ground systems and test sets did occur. Several flights with the early breadboard receiver established that incompatibilities did exist and that they were not correctable by equipment adjustments while in-the-air.

It was then decided by AEL and NASA that the approach would be to utilize a wide bandwidth high speed instrumentation recorder to record the DPSK and log video information, while airborne, and modify the processor to perform on the recorded data. A key to this debugging process was to utilize an AEL Computer-Recorder Interface (CRI) digitizer/mass buffer equipment to convert the wideband analog data into digital data and read it out at a rate compatible with minicomputer I/O interface rate. This process was highly successful, and allowed signal processing and display of the various real intercepted ground signals shown within this portion.

Compatibility of Air/Ground Systems

On April 25, May 3, and June 23, a series of flight tests were conducted by AEL at NAFEC utilizing the LCMLS receiver S/N 002, remote RF head S/N 003, and a SANGAMO SABRE III data recorder mounted in a Piper Cherokee Six aircraft owned by NARCO Scientific Ind., Inc.

The data recording set-up, as depicted in Figure 68, was used for all flight tests with the SABRE III recorder operating in its FM record mode, providing a DC to 250 KHz bandwidth, for both the Discriminator (DPSK) output and the Log Video (TO-FRO) output. The approach paths were, in all cases, straight in from a maximum of 5.5 nm except for the June 23rd run on runway 8. This 5.5 nm range restriction was to prevent approaches over the Atlantic Ocean.

Figure 69 is a plan view of the NAFEC facility for the April 25th and May 3rd flights with the principal MLS sites located as follows: 1) Bendix Basic Narrow (channel 99) on runway 31 and 2) Texas Instruments small community (channel 96 on runway 26. Figure 70 is a plan view of the June 25th situation with the MLS sites arrayed as follows: 1) Bendix Basic Wide (channel 130) on runway 31, 2) Bendix Small Community (channel 197) on runway 8 and 3) Texas Instruments small community on runway 26.

The following covers the significant details and data from each flight test.

Texas Instruments small community (TISC) MLS compatibility. - Figure 71 shows a portion of an azimuth function taken on the April 25th flight. The soft switching of the DPSK preamble is evident along with an unusually shaped "TO TEST" pulse. The "TO" pulse is very broad for a 3° beam.

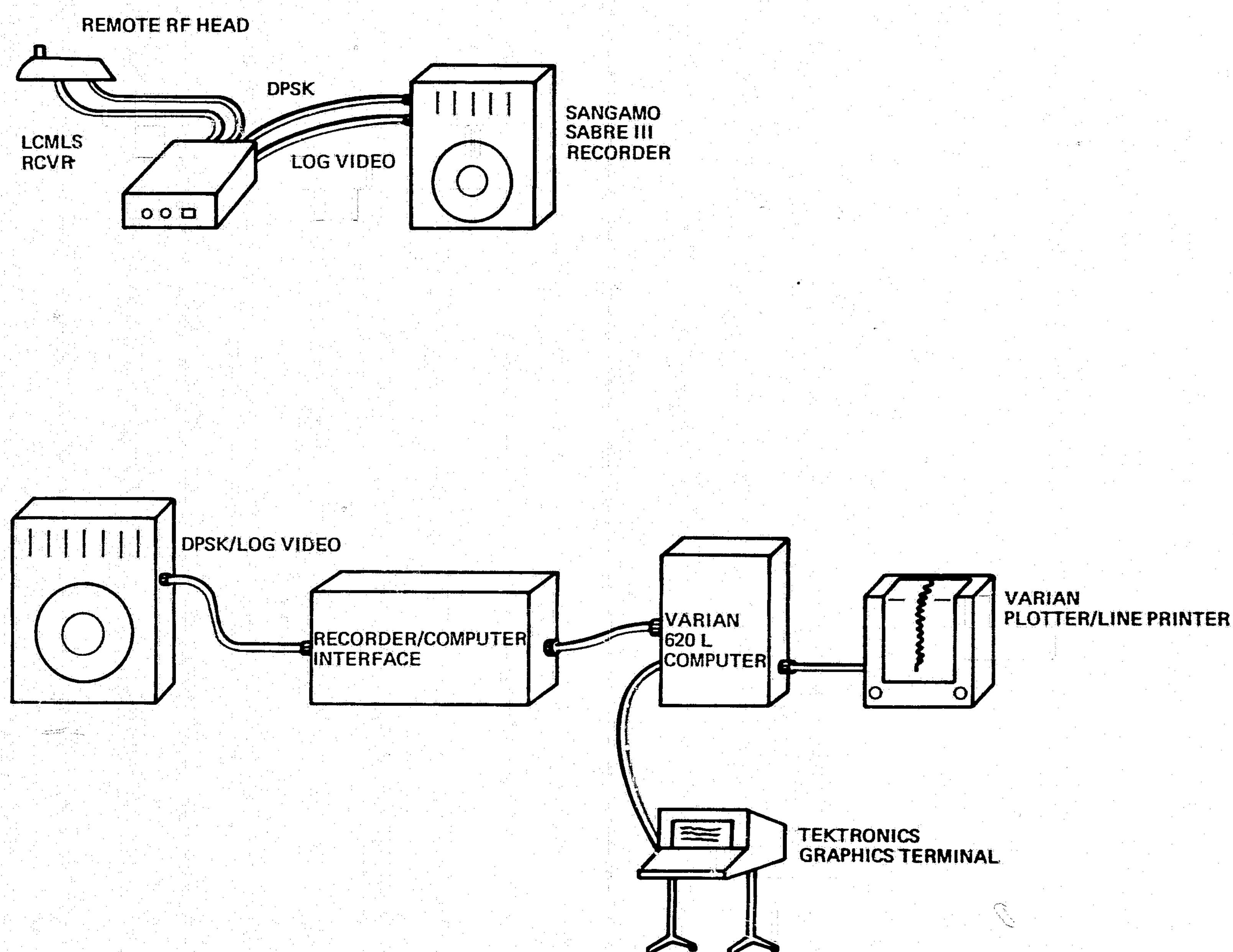


FIGURE 68. PLAYBACK AND ANALYSIS INSTRUMENTATION

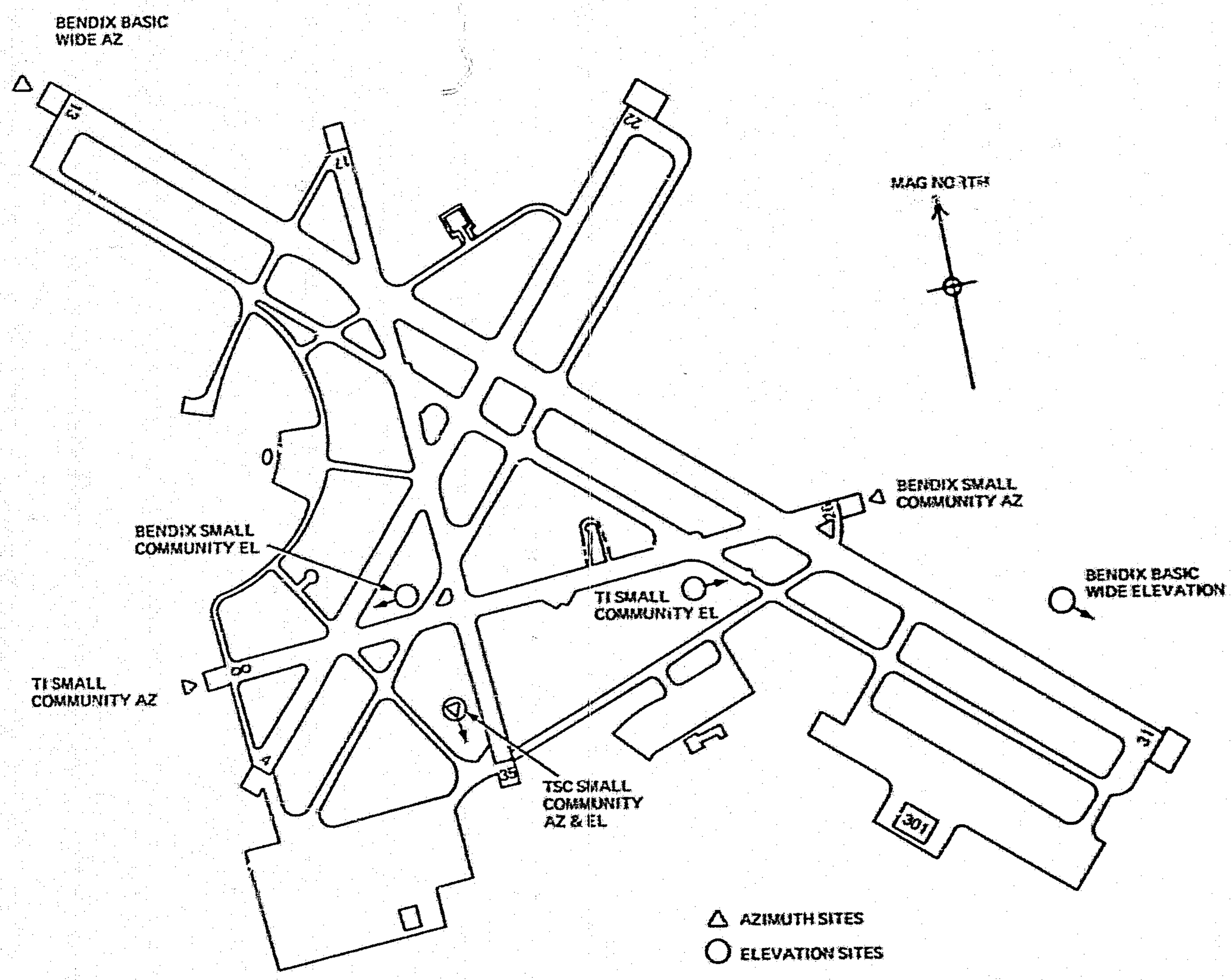


FIGURE 69. NAFEC MLS LAYOUT APRIL 25 AND MAY 3 1978

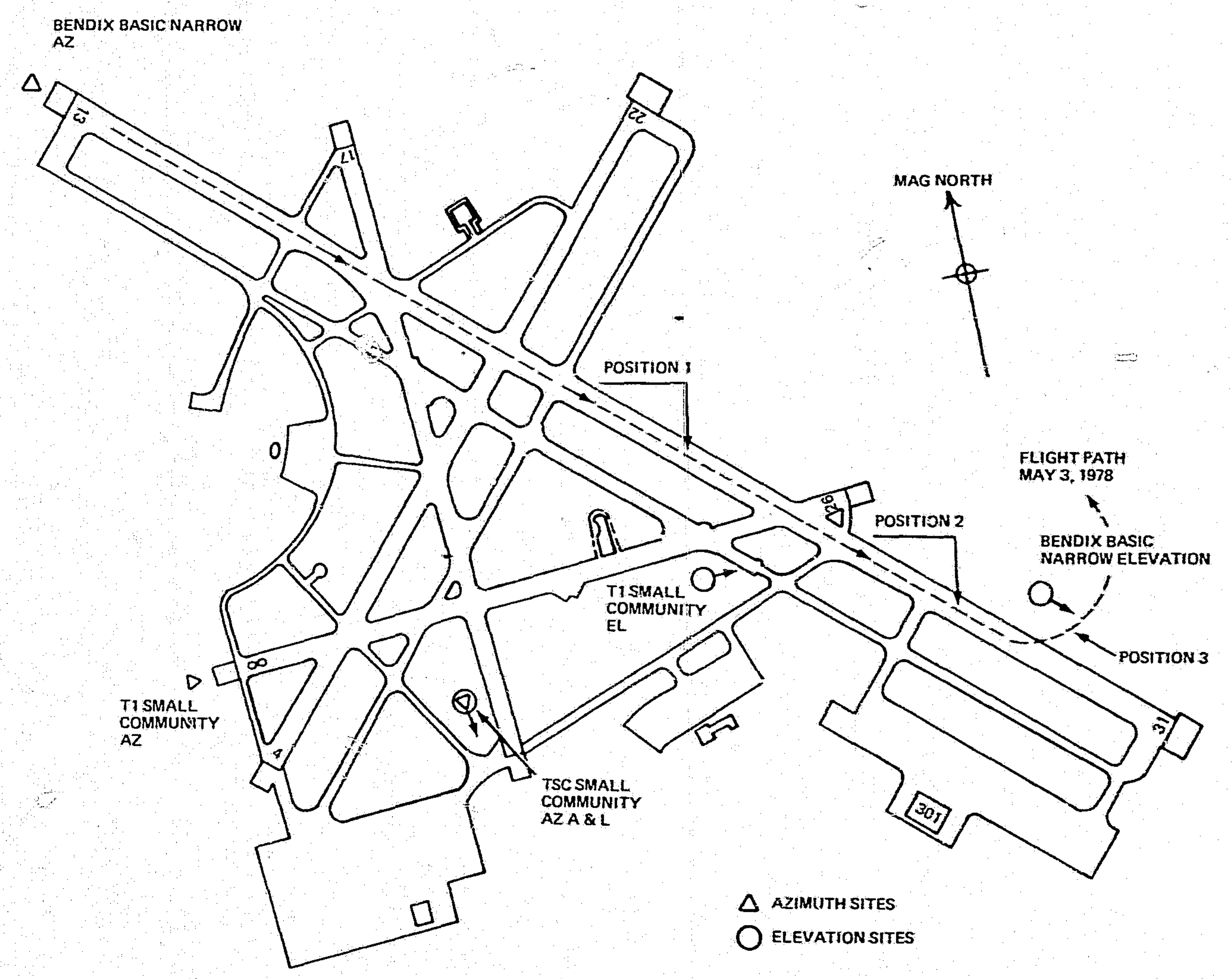
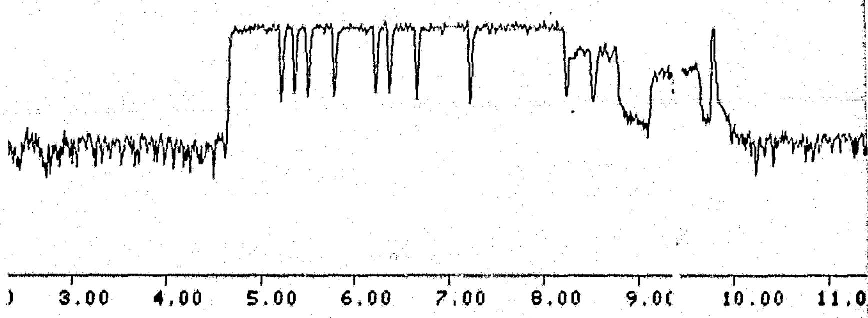


FIGURE 70. NAFEC MLS LAYOUT JUNE 23, 1978

TI SMALL COMMUNITY LOG AMP-
LITUDE

Azimuth Function April 25, 1978

Note variable amplitude guid-
ance pulses and unusual shape
of "To Test" pulse. Very broad
"To" pulse.



FOLDOUT FRAME

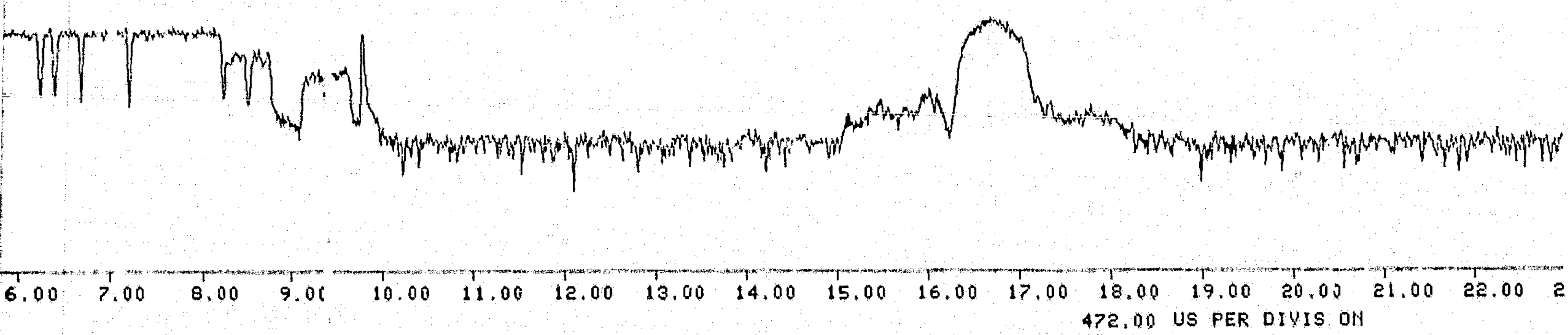


FIGURE 71. TI SMALL COMMUNITY LOG AMPLITUDE

FOLDOUT FRAME 2

The upper portion of Figure 72 shows the Log Video response for Data words 1 and 2 and a portion of an auxiliary data word.. Note the soft switching and propeller modulation envelope. The lower portion of Figure 72 shows the Discriminator response to the soft switched DPSK to be irregular. Figure 73 is a complete elevation function approximately 1 mile from the threshold of runway 26. Notice the lobes of energy in the outsides of the proportional guidance pulses. These are suggestive of an up-down sweep rather than a down-up sweep.

The TI Small Community System was not operating for the May 3rd flight.

Figure 74 shows the Log Video output for the Data words and auxiliary data words and an evaluation function on June 23rd. Notice that the DPSK is now hard switched. The side lobes on the elevation proportional guidance signals suggest a down-up system. The data recorded for Figure 74 was taken at 600 feet altitude at 0.5 nm from threshold of runway 26.

Figure 75 shows a more consistent discriminator response to the hardswitched DPSK. The data for Figure 75 was taken at 2.5 nm from runway 26.

During the flight of June 23rd against the TISC System, the LCMLS Receiver provided full azimuth and elevation proportional readouts over the complete 5.5 nm approach.

Bendix small community (BSC). - The Bendix Small Community System was available for the June 23rd flight and was installed on runway 8 at NAFEC. Figures 76 and 77 are Log Video outputs showing the azimuth function and the elevation and data word #1 respectively. It is interesting to note that the BSC System only transmits one data word. The lack of data word #2 causes the LCMLS receiver to flag its elevation outputs as it does not receive an MLS ground status update for elevation. For this flight test however, the program memory in the LCMLS Receiver Processor was modified to ignore the lack of this data.

Figure 78 shows the discriminator response to the BSC DPSK signals for data word #1 and the elevation preamble. This response is considered adequate.

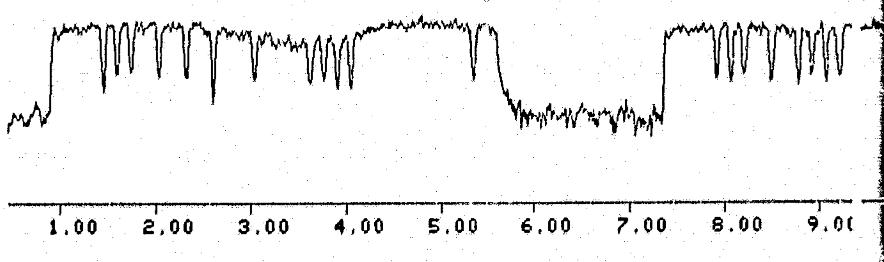
The LCMLS receiver provided continuous azimuth and elevation proportional guidance over a 5 nm approach to landing against the Bendix Small Community System.

Bendix basic narrow (BBN). - The Bendix Basic Narrow System was operating in azimuth only on April 25th and since the graphed data for that run is similar to the May 3rd run, it is not included herein.

Figure 79 is a Log Video presentation of the elevation and azimuth functions at 5.25 nm and 2500 feet altitude. The variations in "Down-up" and "TO-FRO" pulses is most probably propeller modulation. Note that the elevation preamble is weaker than azimuth.

TI SMALL COMMUNITY LOG AMPLITUDE

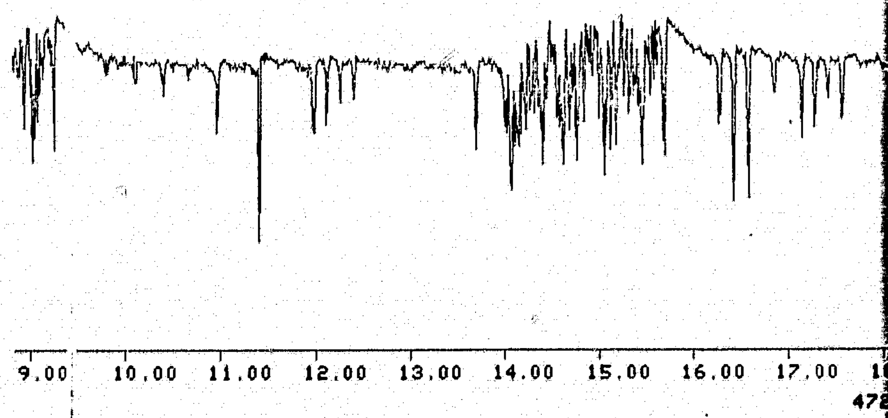
Data Word #1, #2, Aux Data



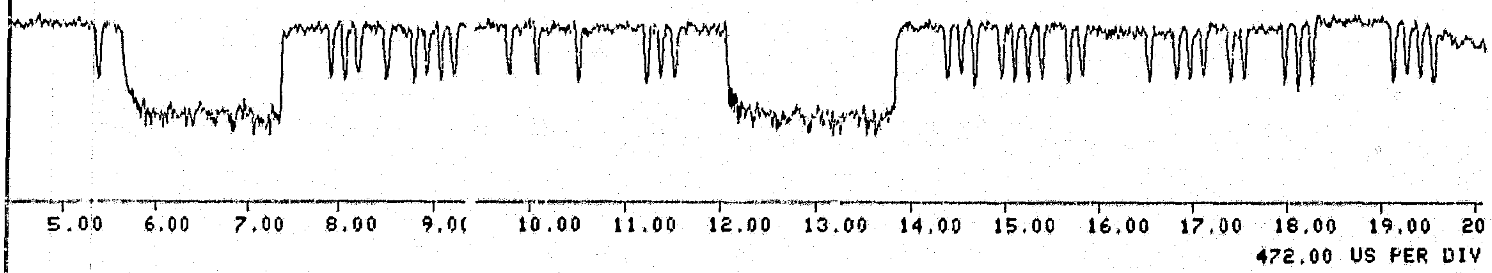
TI SMALL COMMUNITY DISCRIMINATOR OUTPUT

Data Word #1, #2, Aux Data

Note absence and irregularity of phase transition detection



FOLDOUT FRAME



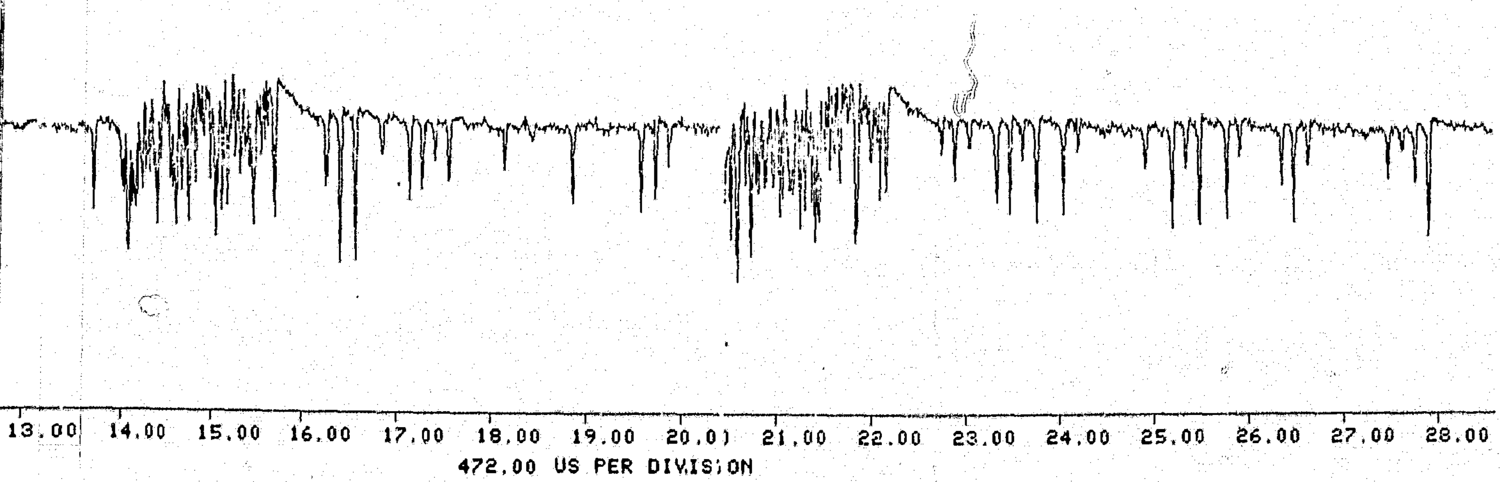
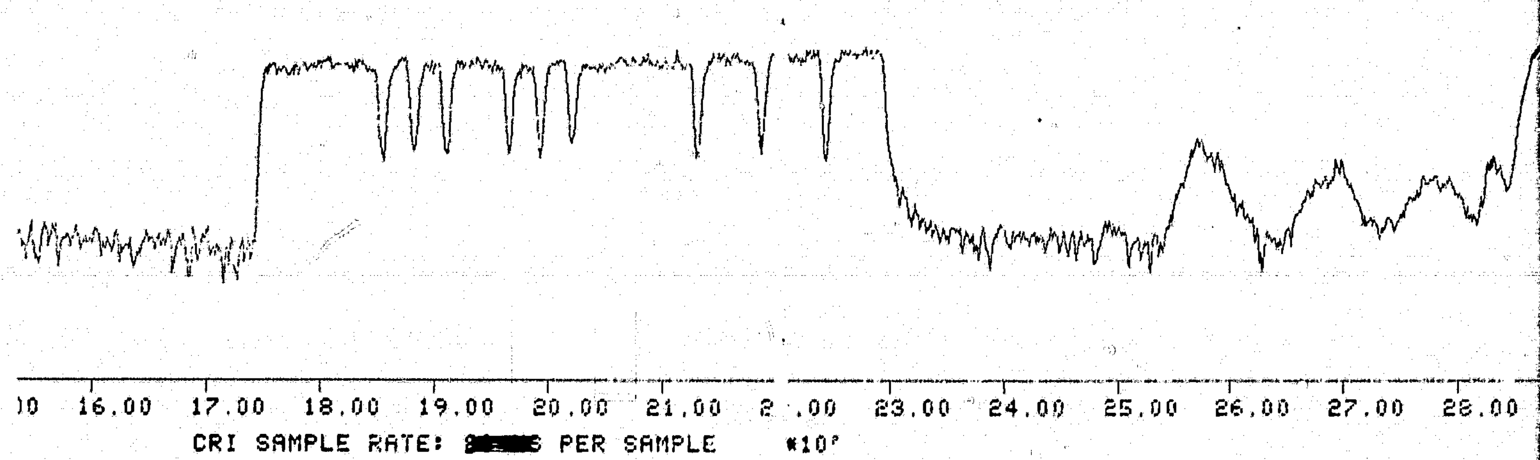
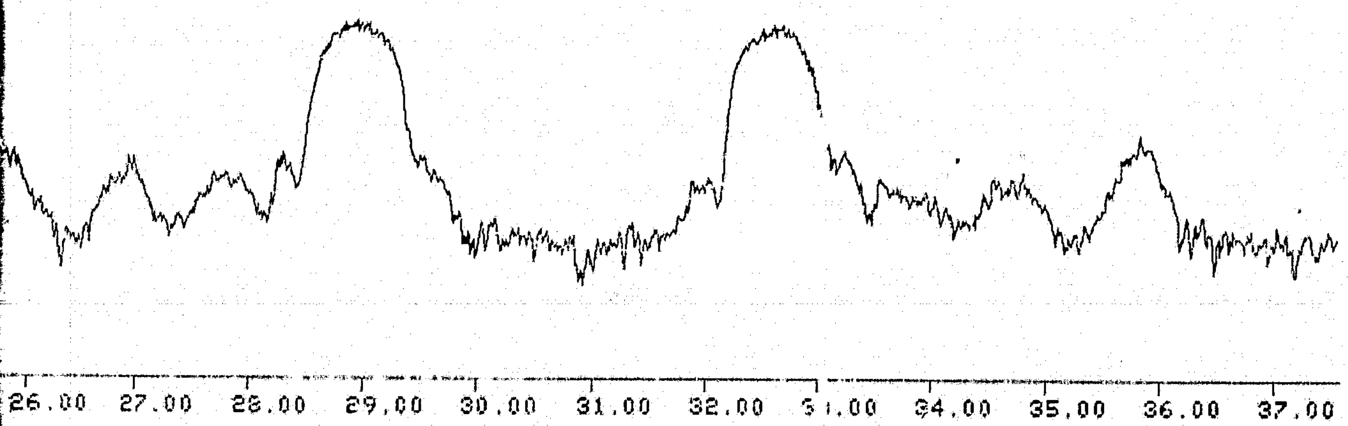


FIGURE 72. TI SMALL COMMUNITY DISCRIMINATOR OUTPUT

FOLDOUT FRAME 2

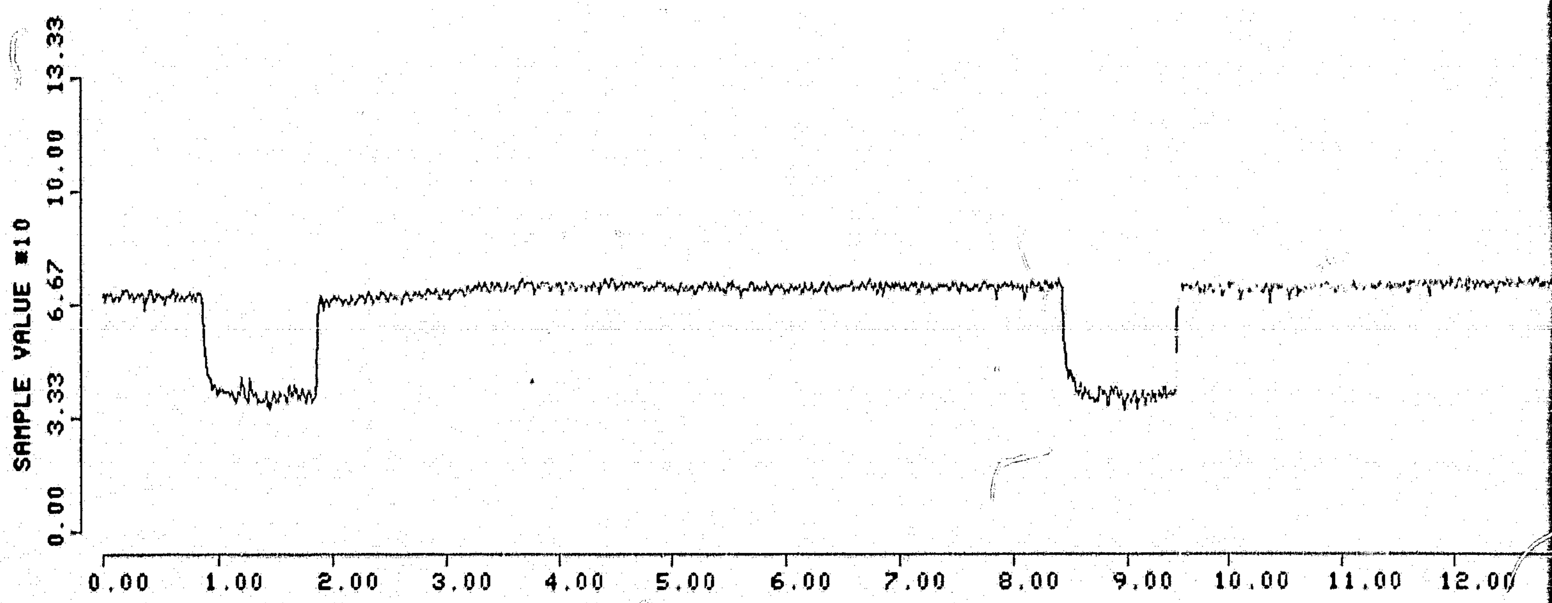


FOLDOUT FRAME



FOLDOUT FRAME 2

FIGURE 73. TI SMALL COMMUNITY LOG AMPLITUDE ELEVATION FUNCTION, 1.0 NM FROM RNWY 26, 4-25-78



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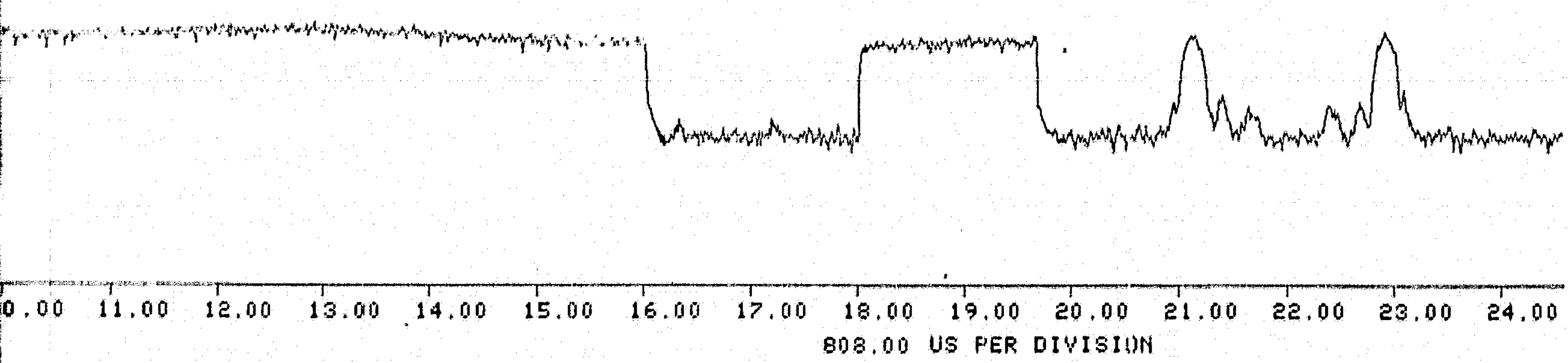
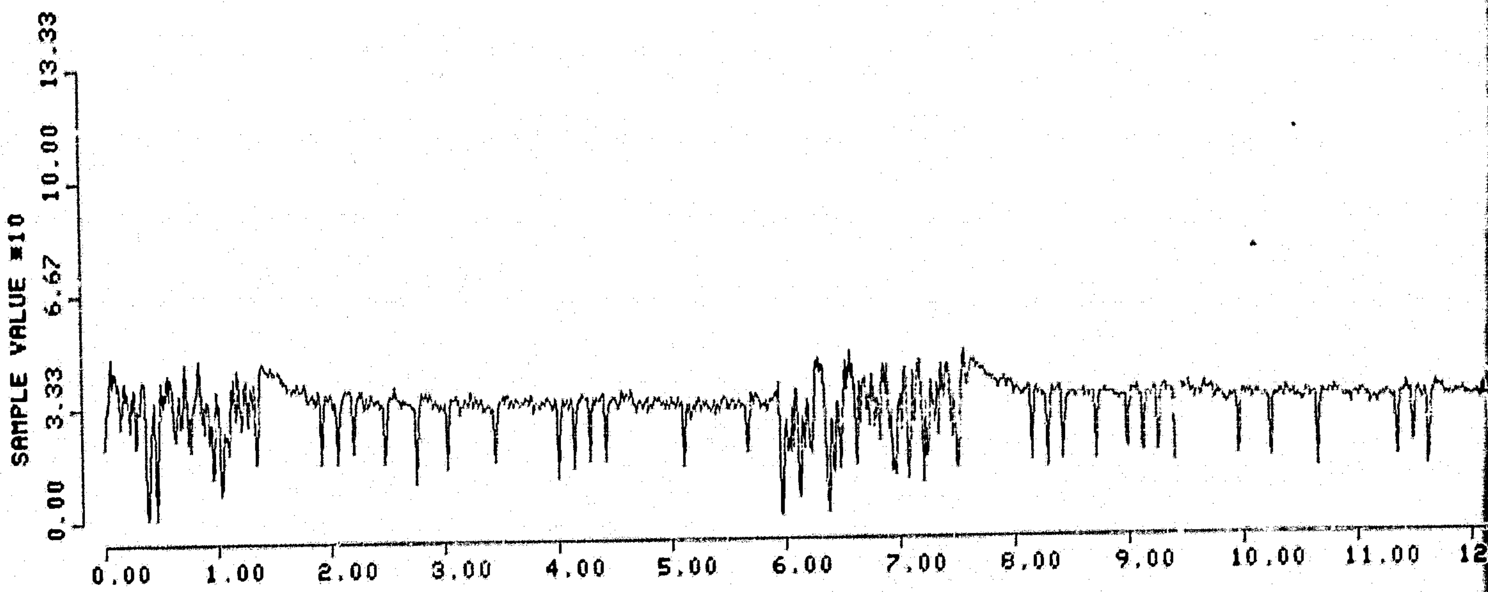
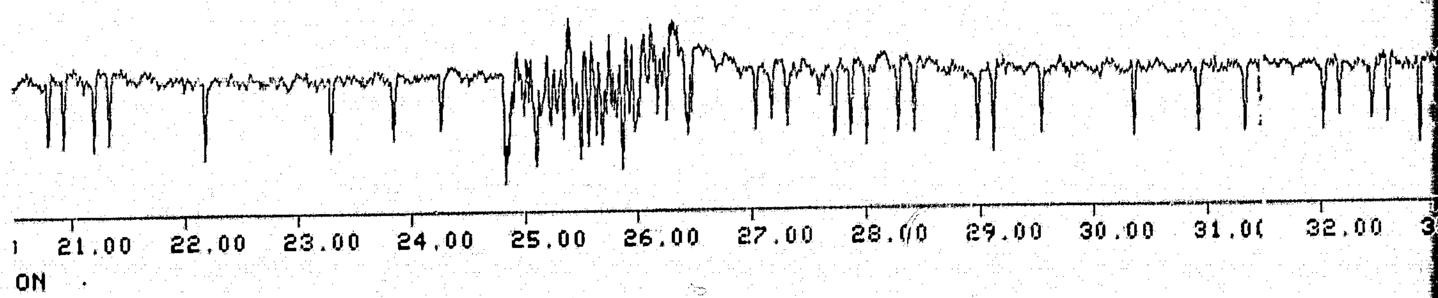


FOLDOUT FRAME 2

FIGURE 74. TI SMALL COMMUNITY LOG AMPLITUDE AUX DATA WORDS AND ELEVATION FUNCTION, 0.5 NM FROM RNWY 26, 6-23-78





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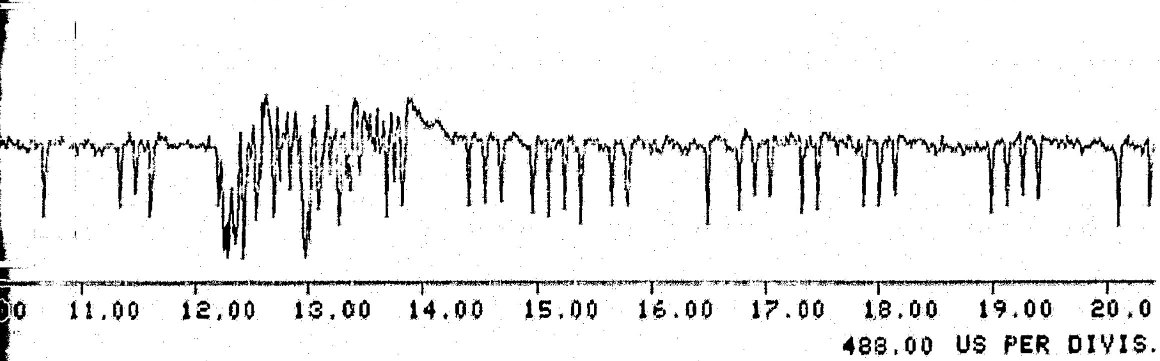


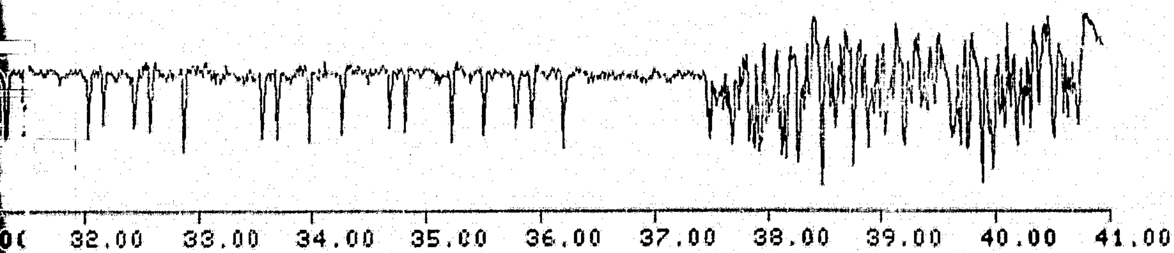
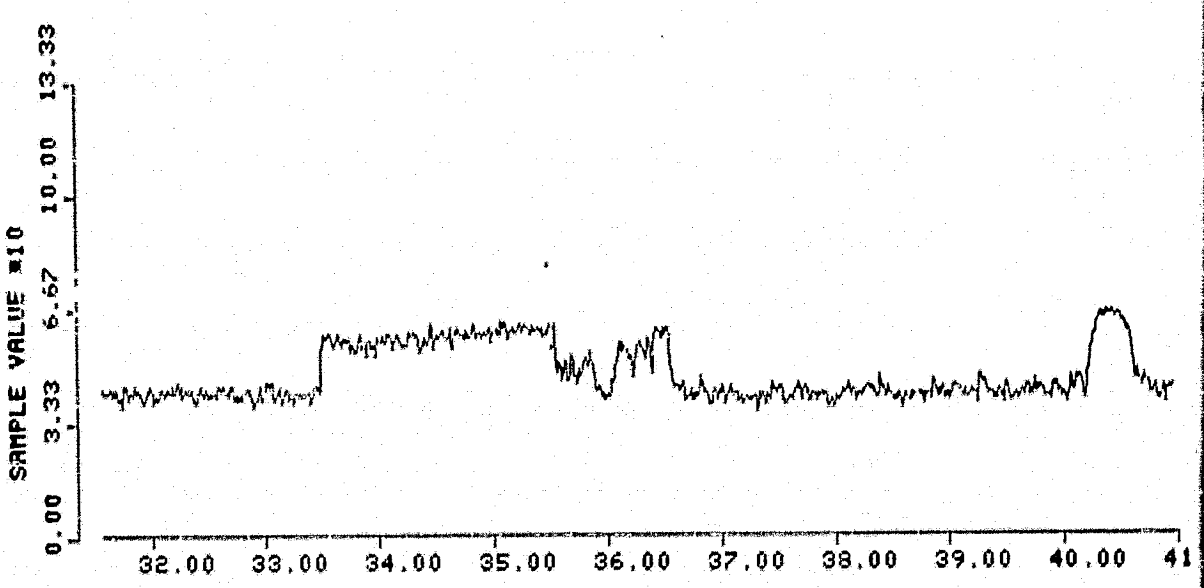


FIGURE 75. TI SMALL COMMUNITY RECOVERED DPSK DATA AND AUX DATA WORDS, 2.5 NM FROM RNWY 26, 6-23-78

FOLDOUT FRAME 2



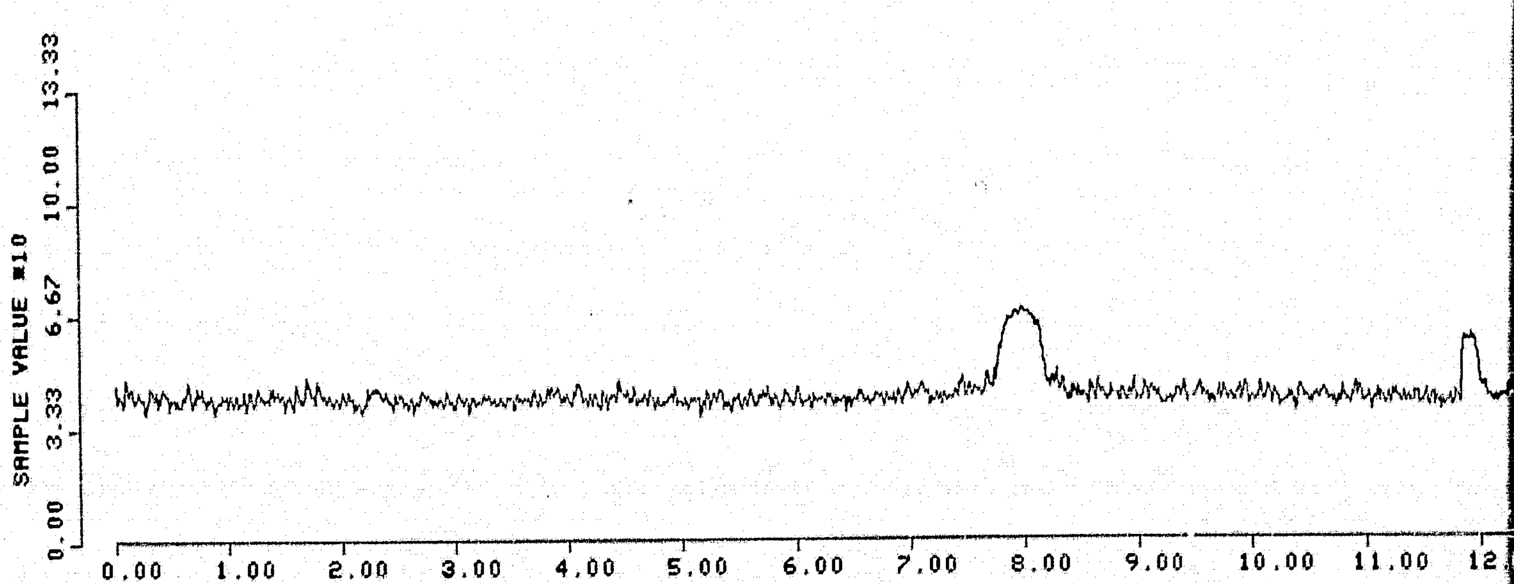


FIGURE 76. BENDIX S
AMPLITUDE AZ
1 NM FROM R

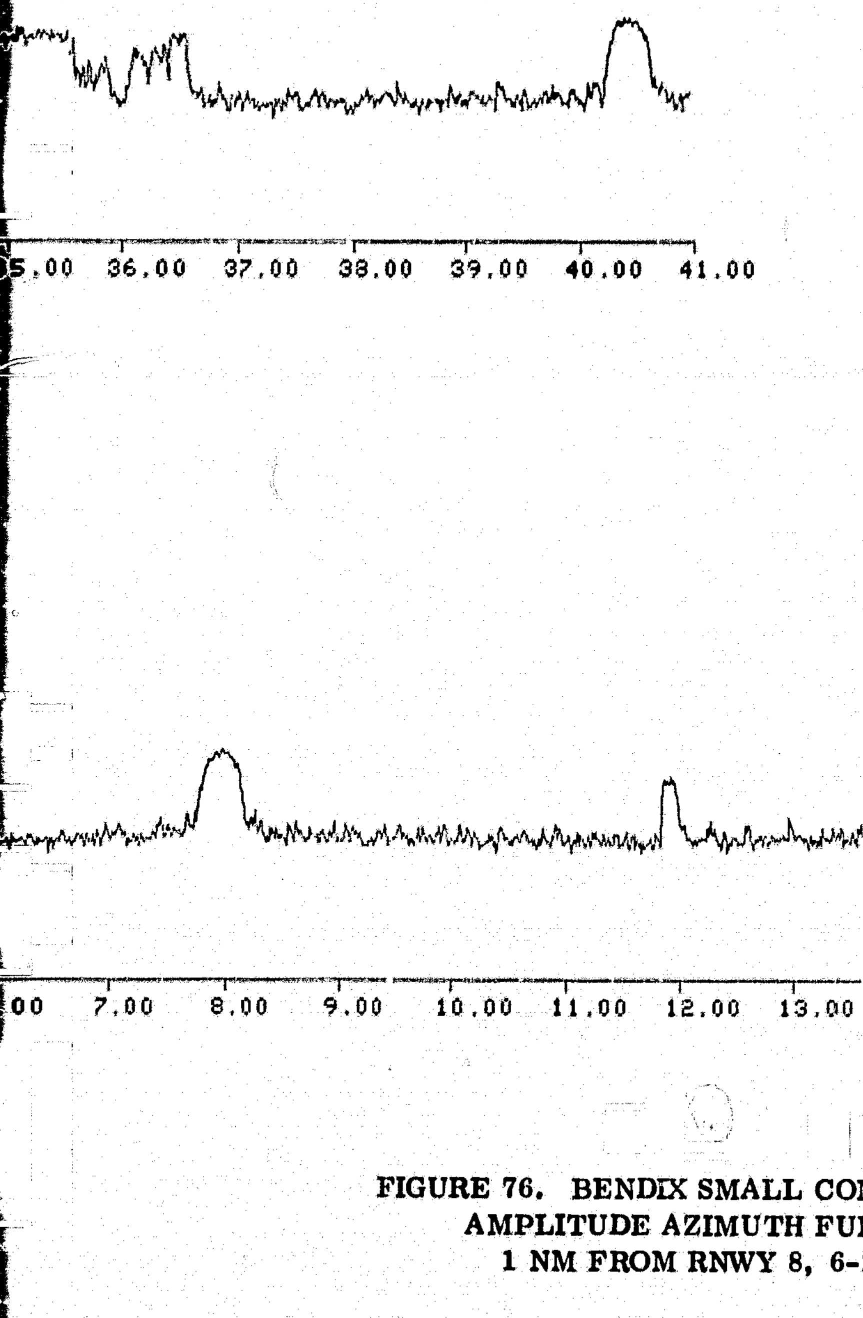
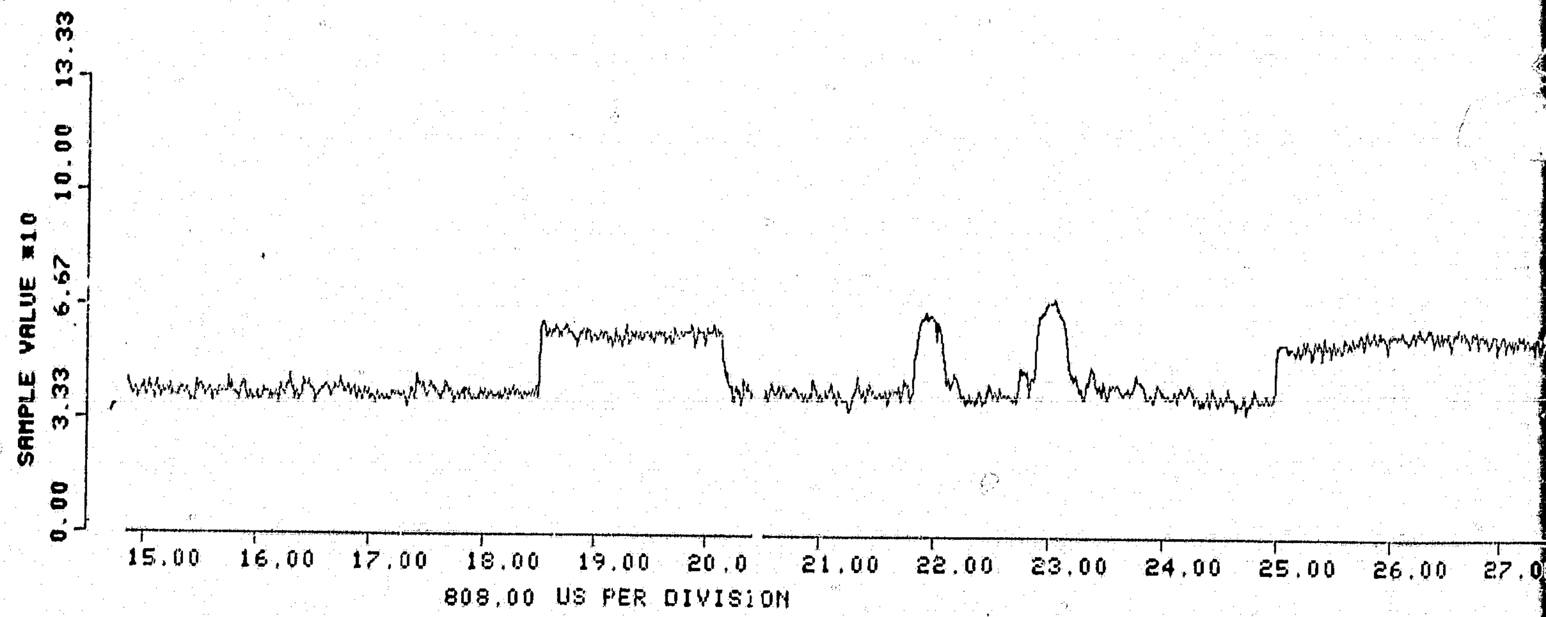


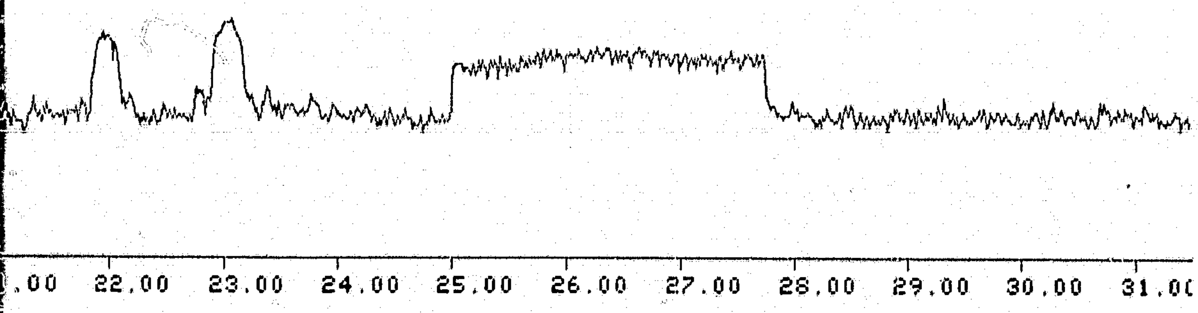
FIGURE 76. BENDIX SMALL COMMUNITY LOG AMPLITUDE AZIMUTH FUNCTION, 1 NM FROM RNWY 8, 6-23-78

FOLDOUT FRAME



FOLDOUT FRAME

FIGURE 7
AMPLIT
FUN



FOLDOUT FRAME 2

FIGURE 77. BENDIX SMALL COMMUNITY LOG AMPLITUDE ELEVATION AND DATA WORD FUNCTIONS, 0.1 NM FROM RNWY 8, 6-23-78

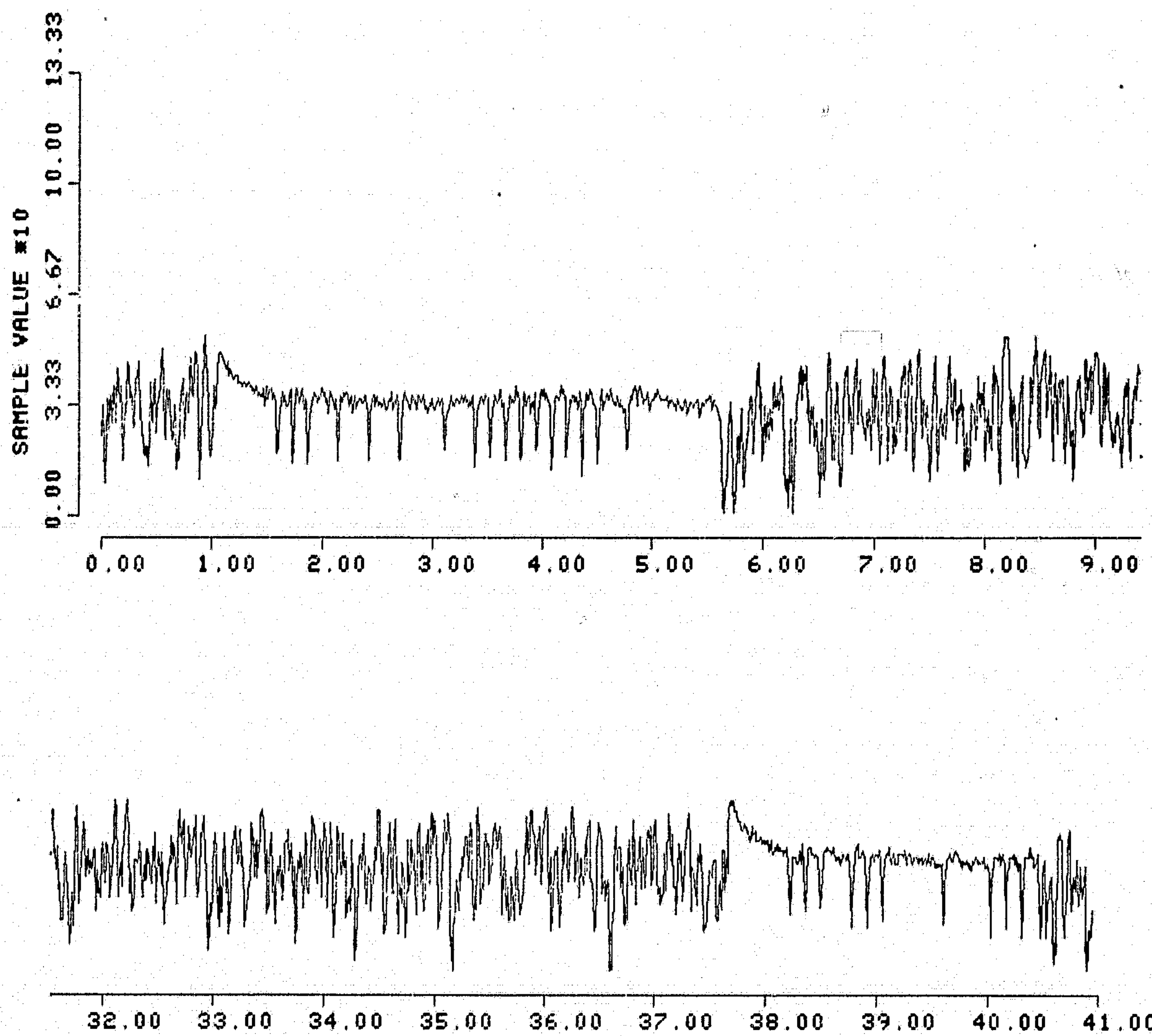
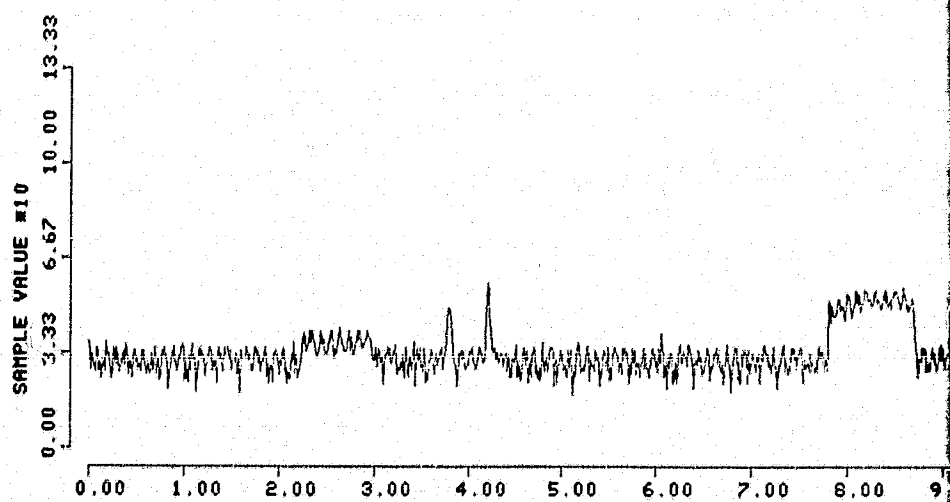


FIGURE 78. BENDIX SMALL COMMUNITY RECOVERED DPSK DATA WORD #1 AND ELEVATION PREAMBLE, 2 NM FROM RNWY 8, 6-23-78

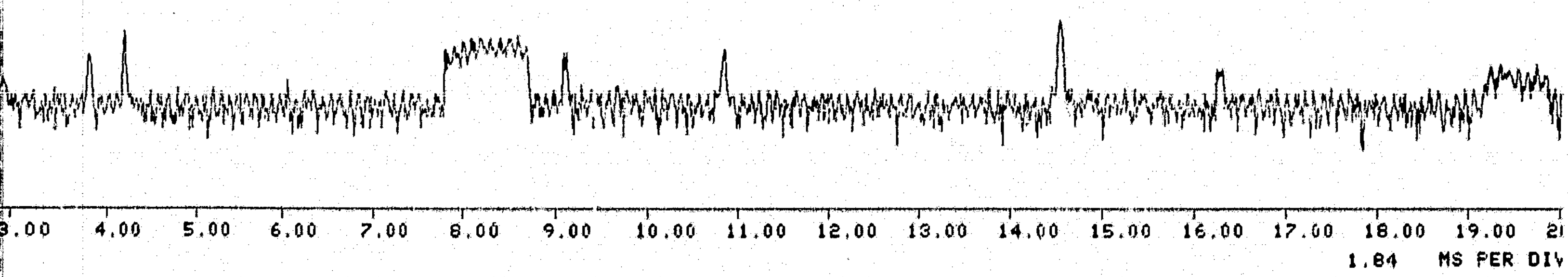
BENDIX BASIC NARROW LOG AMPLITUDE

Data at 5.25 nm. & 2500 ft. alt.

Note difference in elevation signal strength (left) vs Azimuth (middle)



FOLDOUT FRAME



FOLDOUT FRAME 2

FIGURE 79. BENDIX BASIC NARROW
LOG AMPLITUDE

Figure 80 depicts the elevation function and an auxiliary data word at 3 nm on runway 31. Note the propeller modulation envelope on the auxiliary data word.

Although the LCMLS receiver did not respond in an adequate fashion to these signals on May 3rd the tapes facilitated the troubleshooting and the appropriate modifications were made to the LCMLS receiver such that it would reliably "fly the tape" for the full 5 nm.

On May 3rd a low approach was made on runway 13 which is opposite the operating direction of the MLS System on runway 31. In this case the LCMLS receiver was "Looking over the tail" at the azimuth antenna. Proportional guidance was received as the aircraft proceeded along runway 13. Between position 1 and position 2 (see Figure 70) the azimuth signal received decayed into the noise. This is shown in Figure 81 in three successive graphs. At position 3 (Figure 70), in a climbing left turn, the azimuth signal had recovered to give proportional guidance and elevation proportional guidance was also displayed. This is shown in Figure 82.

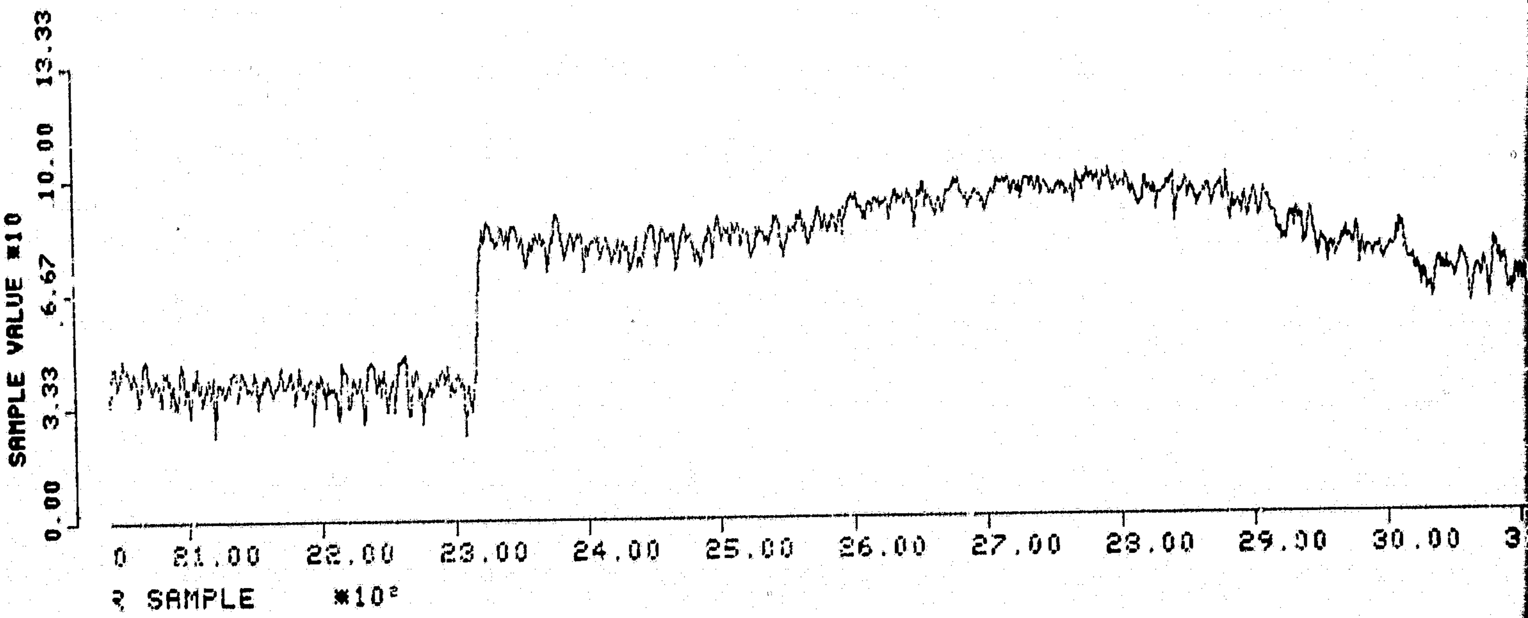
The Bendix Basic Narrow provided a hard switched DPSK format and the LCMLS receiver discriminator output was proper as shown in a previous graph, (Figure 78).

Bendix (BBW). - For the flight test of June 23rd, the Bendix MLS system was installed on runway 31. Although the system was reported to be operational, the elevation function was useless due to a low level signal in space and data words were not evident. The Azimuth Function was also low in power but provided coverage to 3 nm. Figure 83 is a Log Video plot of the Basic Wide System at 5 nm. The proportional guidance beams for elevation and azimuth are sufficient but the preambles, especially elevation, are too low level. Figure 84 is the plot at 1 nm from runway 31. The elevation preamble is still useless. Figure 85 is a graph of the discriminator response to the DPSK signal at 1 nm. Notice that the elevation preamble is noisy and garbled. The LCMLS receiver provided proportional guidance in azimuth at 3 nm and elevation at 0.5 nm.

Hazeltine small community (HSC).- On July 31st, 1978 the LCMLS receiver was operated against the Hazeltine Small Community system installed at Hazeltine Corp's Smithtown Range. The distance between transmitter and receiver was 1000 feet. Because of modifications being added to the Azimuth Assembly it was not possible to operate "Az" and "EL" sites simultaneously.

Figure 86 is the log video response to the elevation signal at approximately a 5° glide slope. Because of the closeness of the transmitter, the transmit pedestal is much in evidence. Note also that the Preamble Phase Transitions are barely visible indicating slightly softer switching than "the hard switched" Bendix MLS transmitters.

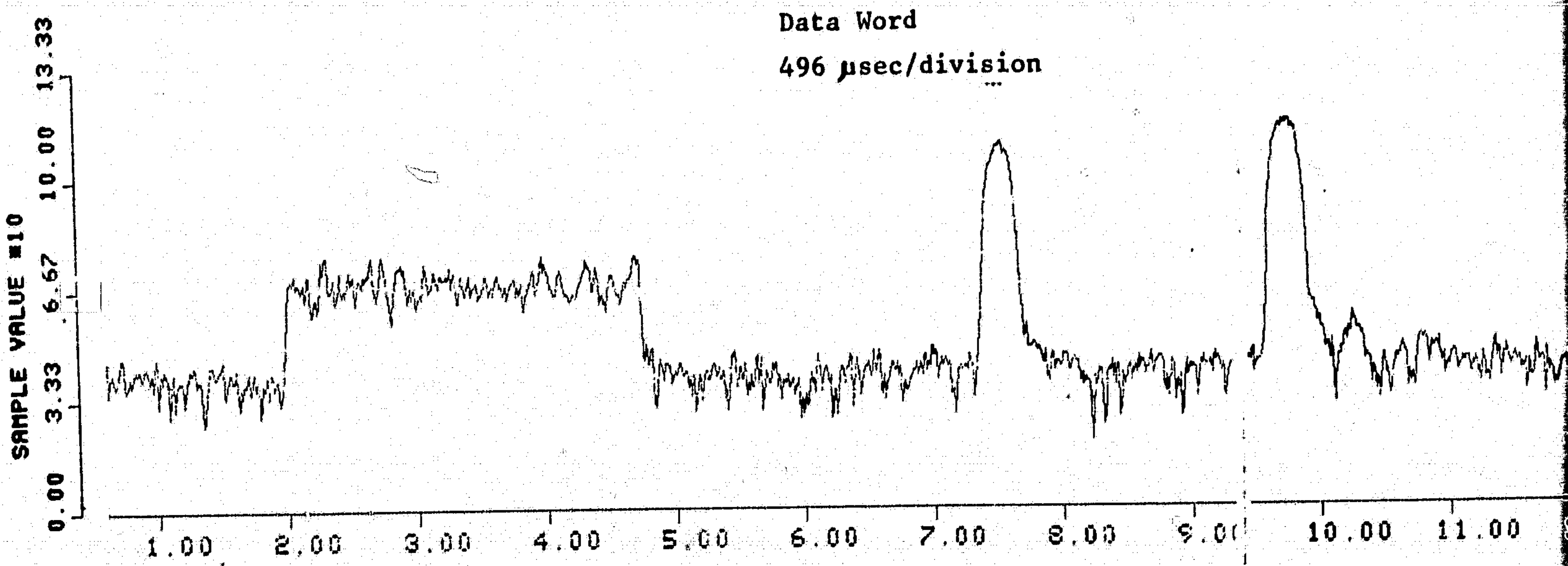
Figure 87 is the Elevation DPSK Preamble as outputted from the discriminator. Note that adjacent phase transitions are unequal. This likely is caused by unbalance in the phase modulator.



Bendix Basic Narrow Log Amplitude

Data Word

496 μsec/division

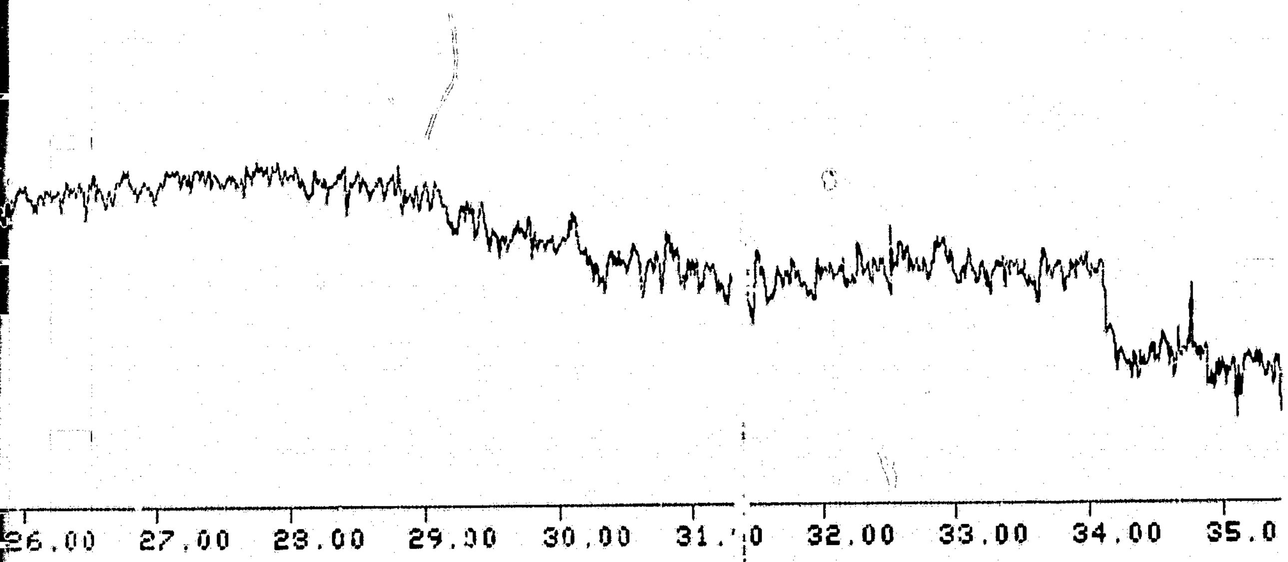


Bendix Basic Narrow Log Amplitude

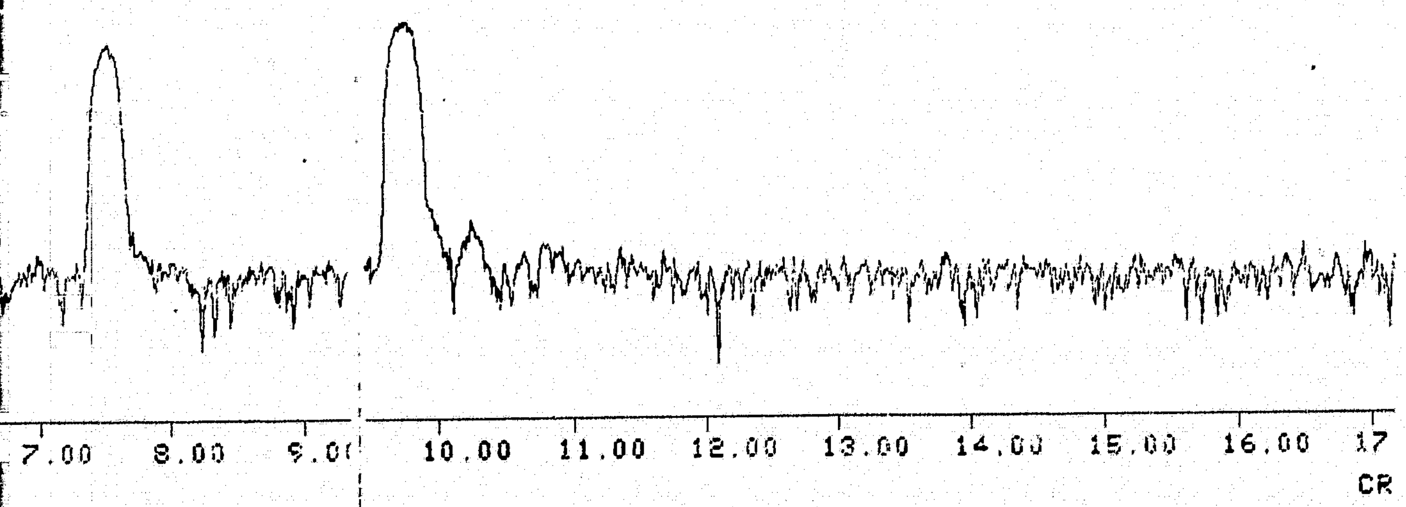
Elevation Preamble/Down/Up

496 μsec/division

FOLDOUT FRAME



asic Narrow Log Amplitude
d
/division



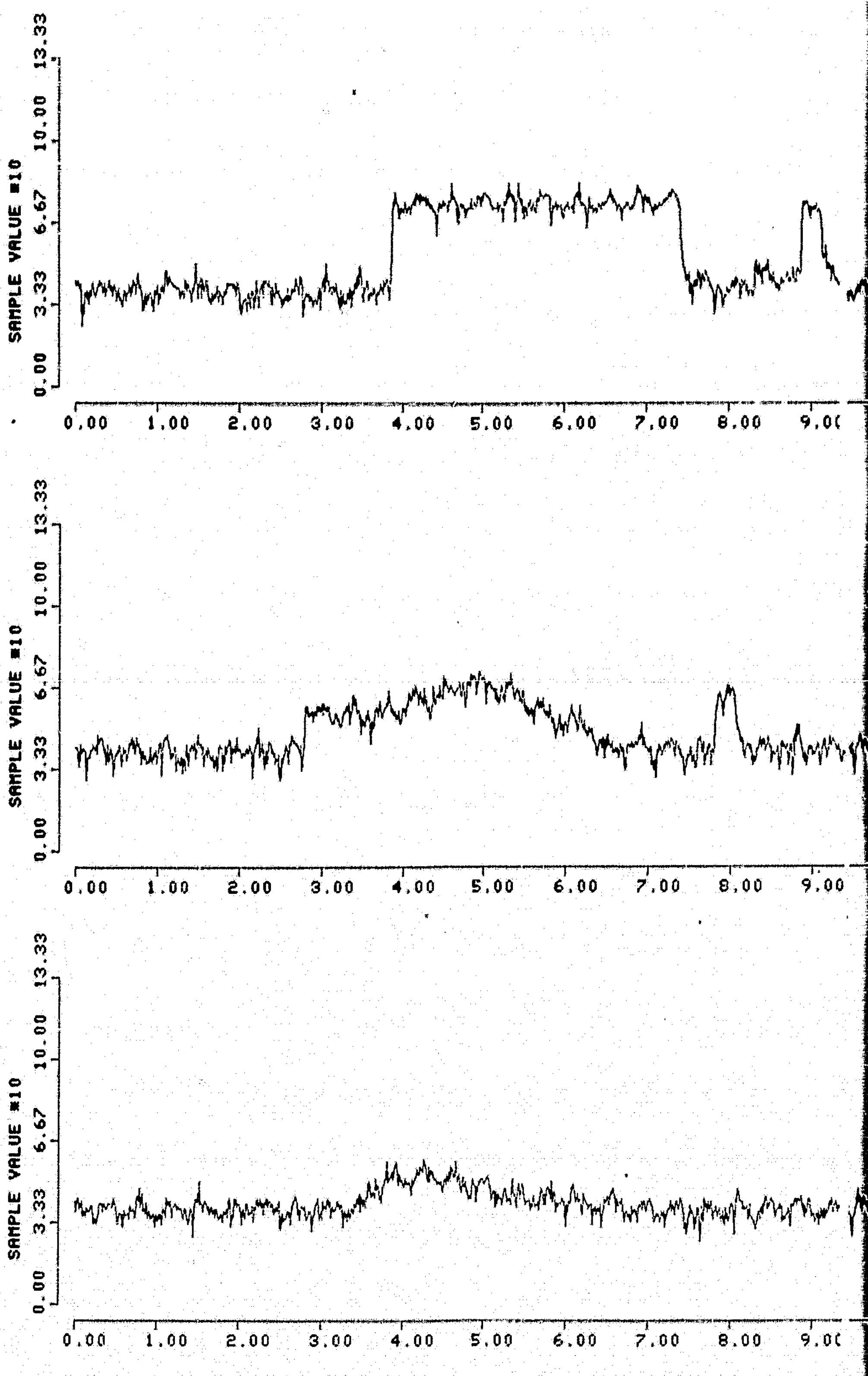
sic Narrow Log Amplitude
Preamble/Down/Up
division

FIGURE 80. BENDIX BASIC NARROW LOG AMPLITUDE DATA WORD

FOLDOUT FRAME 2

BENDIX BASIC NARROW LOG AMPLITUDE

Successive data taken @ 10' altitude along center line of RW 13. Note how signal deteriorates until crossing RW 26 where signal is gone entirely



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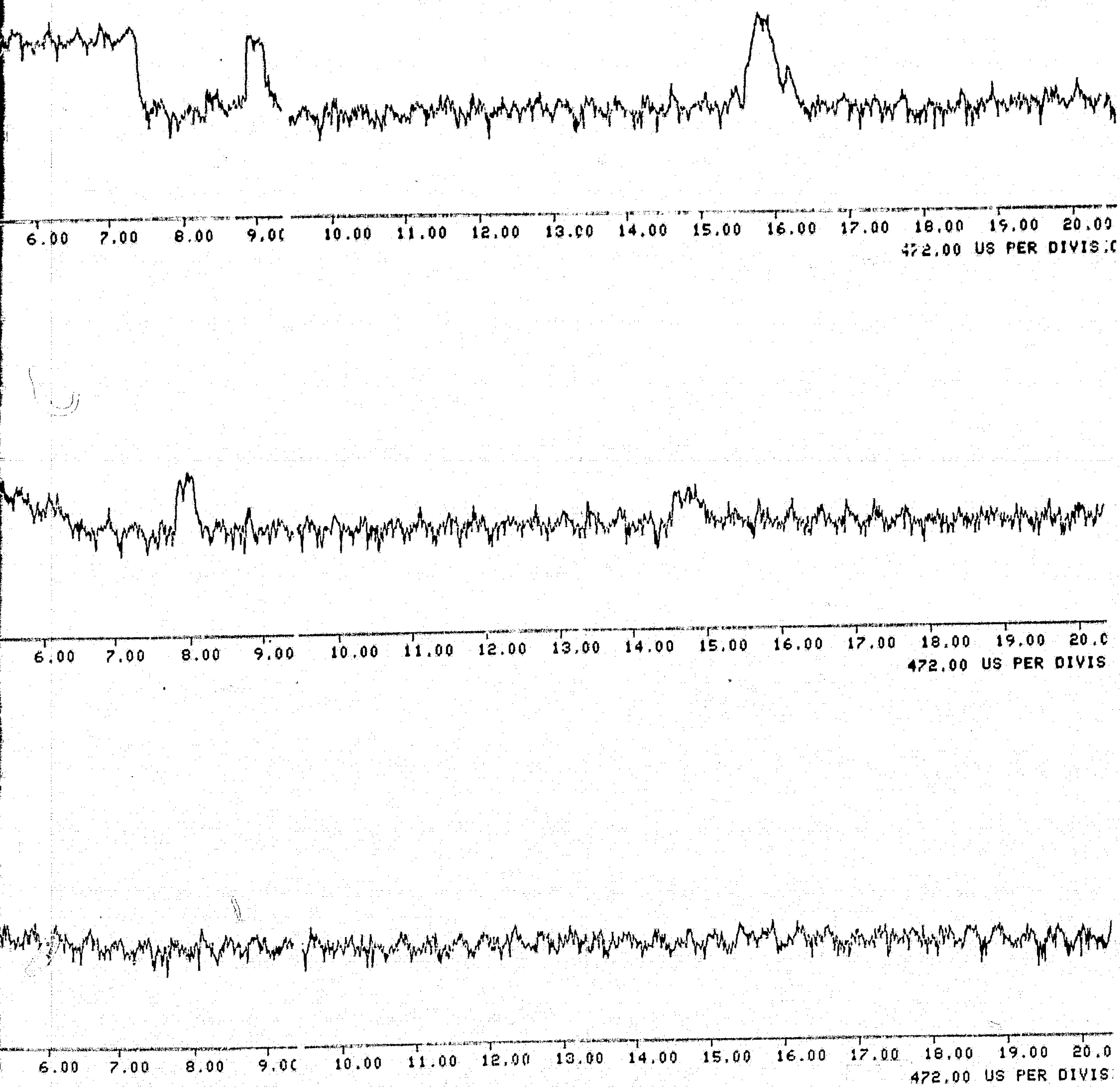
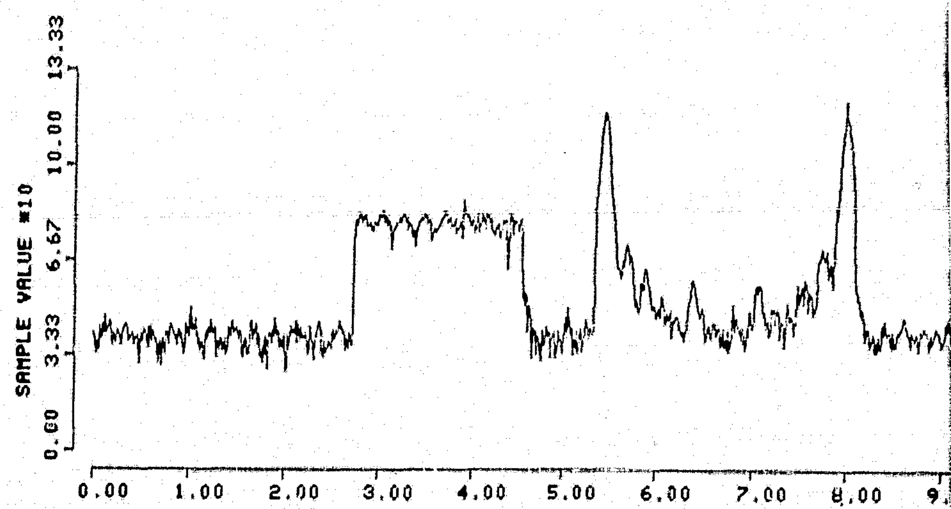


FIGURE 81. BENDIX BASIC NARROW LOG AMPLITUDE

FOLDOUT FRAME 2

BENDIX BASIC NARROW LOG AMPLITUDE

Taken @ 100' altitude in climbing left turn off of RW 13 just past intersection of RW 26 in front of elevation transmitter -large signal amplitude difference between EL & AZ had no detrimental effect on receiver performance



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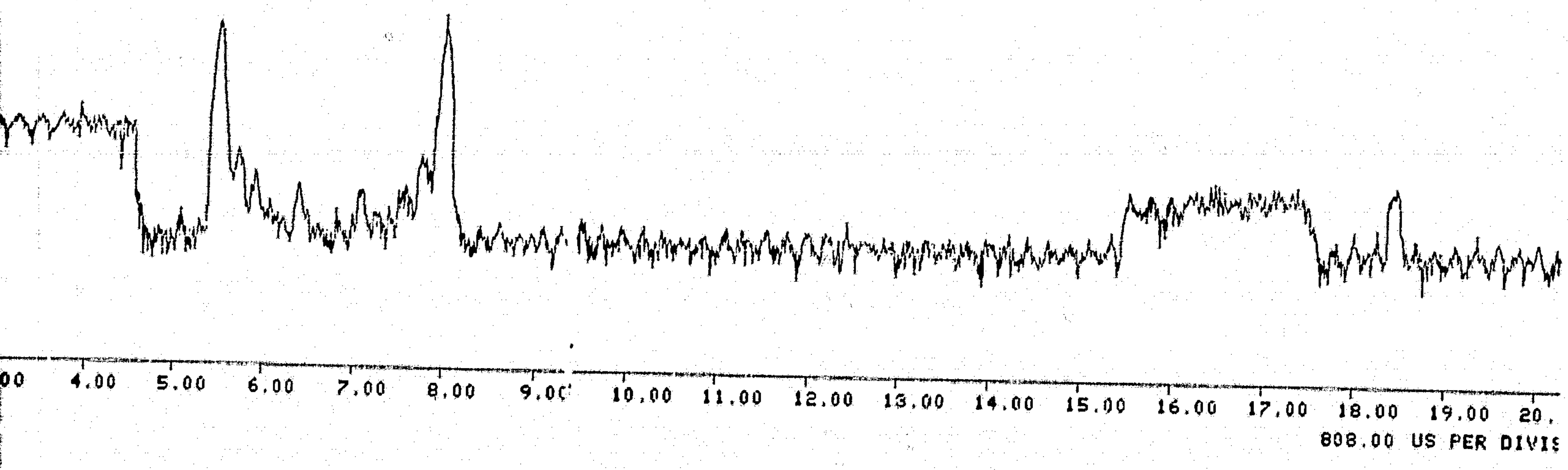

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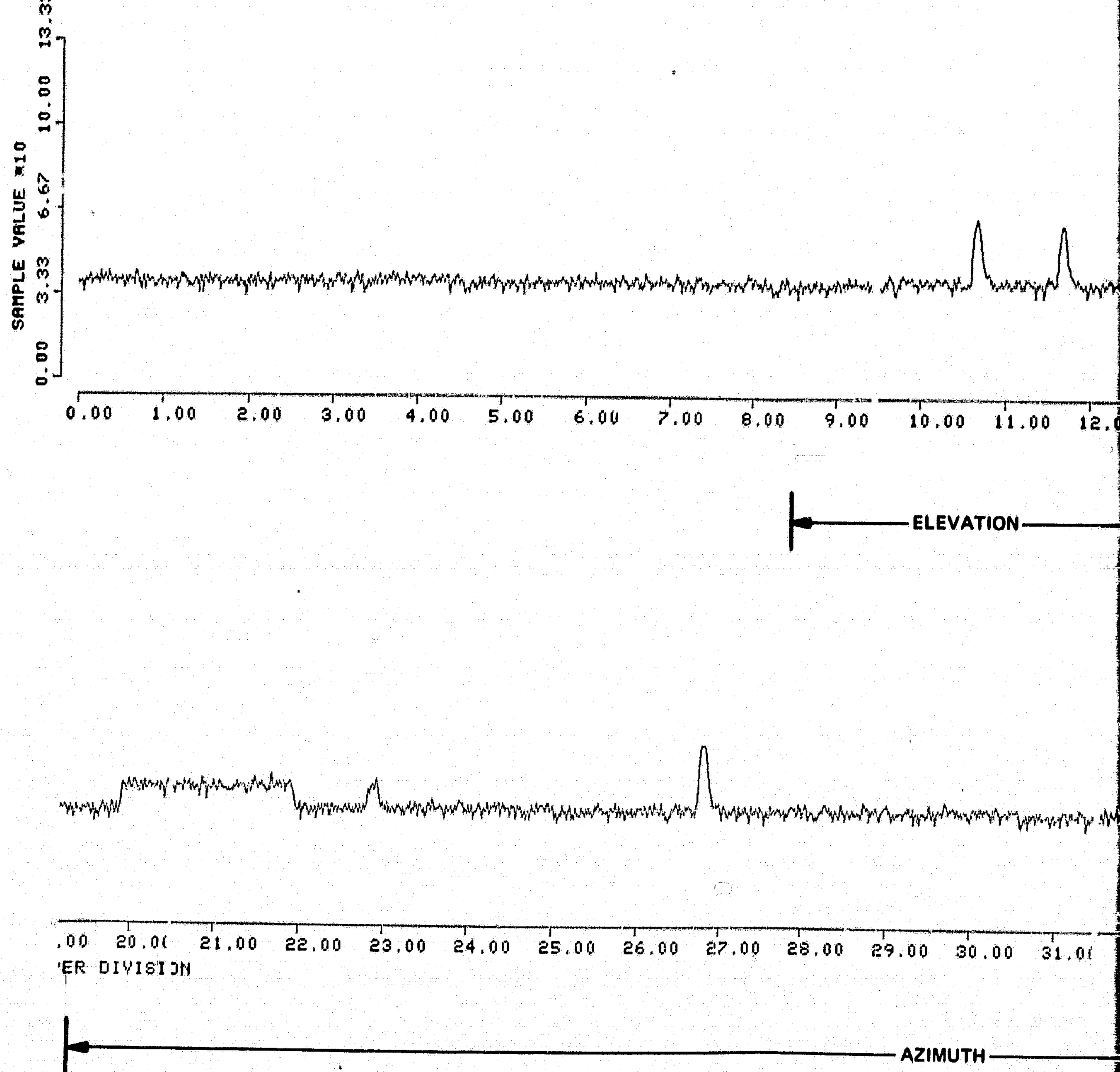
FIGURE 82. BENDIX BASIC NARROW LOG AMPLITUDE



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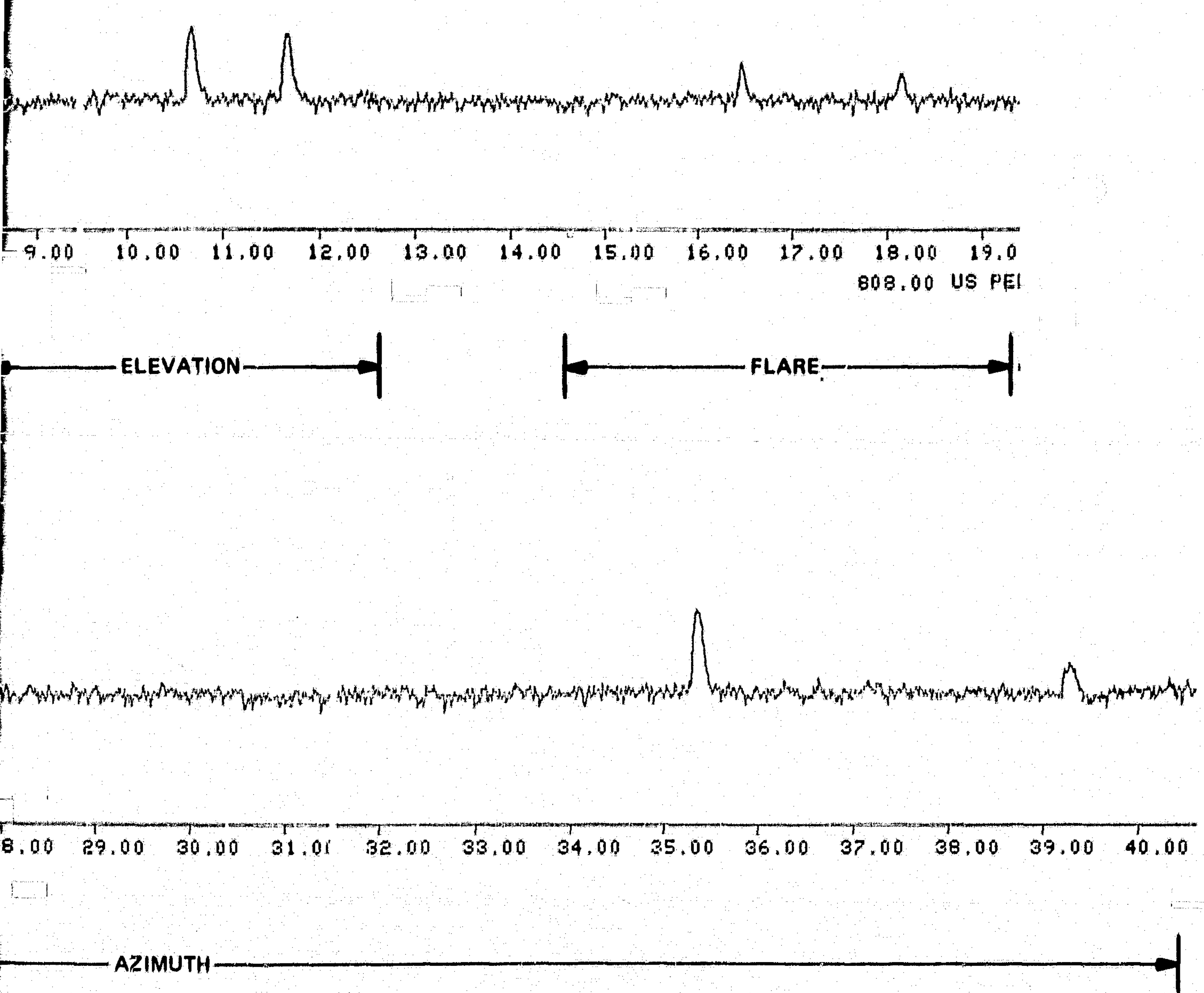
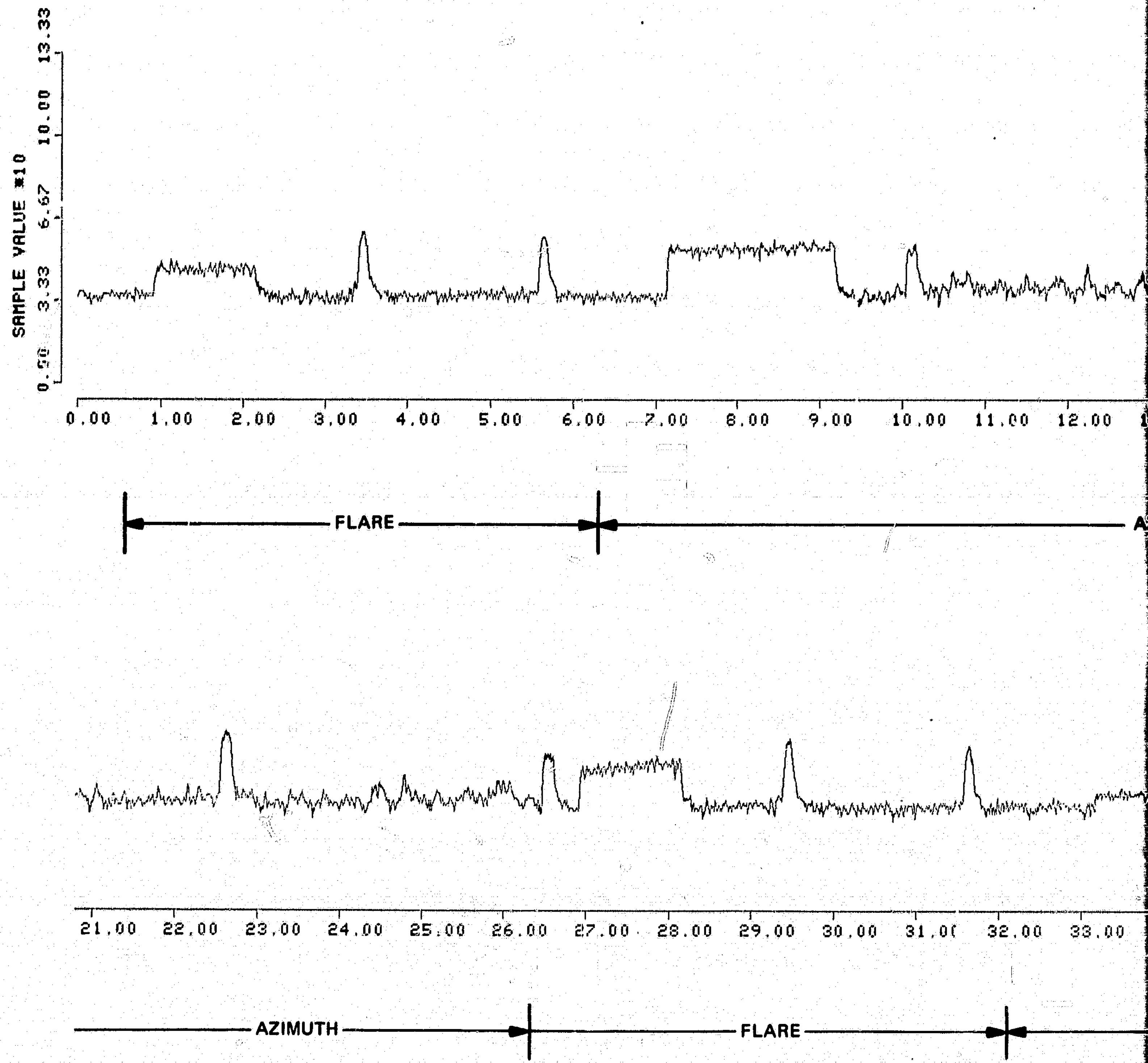


FIGURE 83. BENDIX BASIC WIDE LOG AMPLITUDE PLOT, 5 NM FROM RNWY 31, 6-23-78

FOLDOUT FRAME 2



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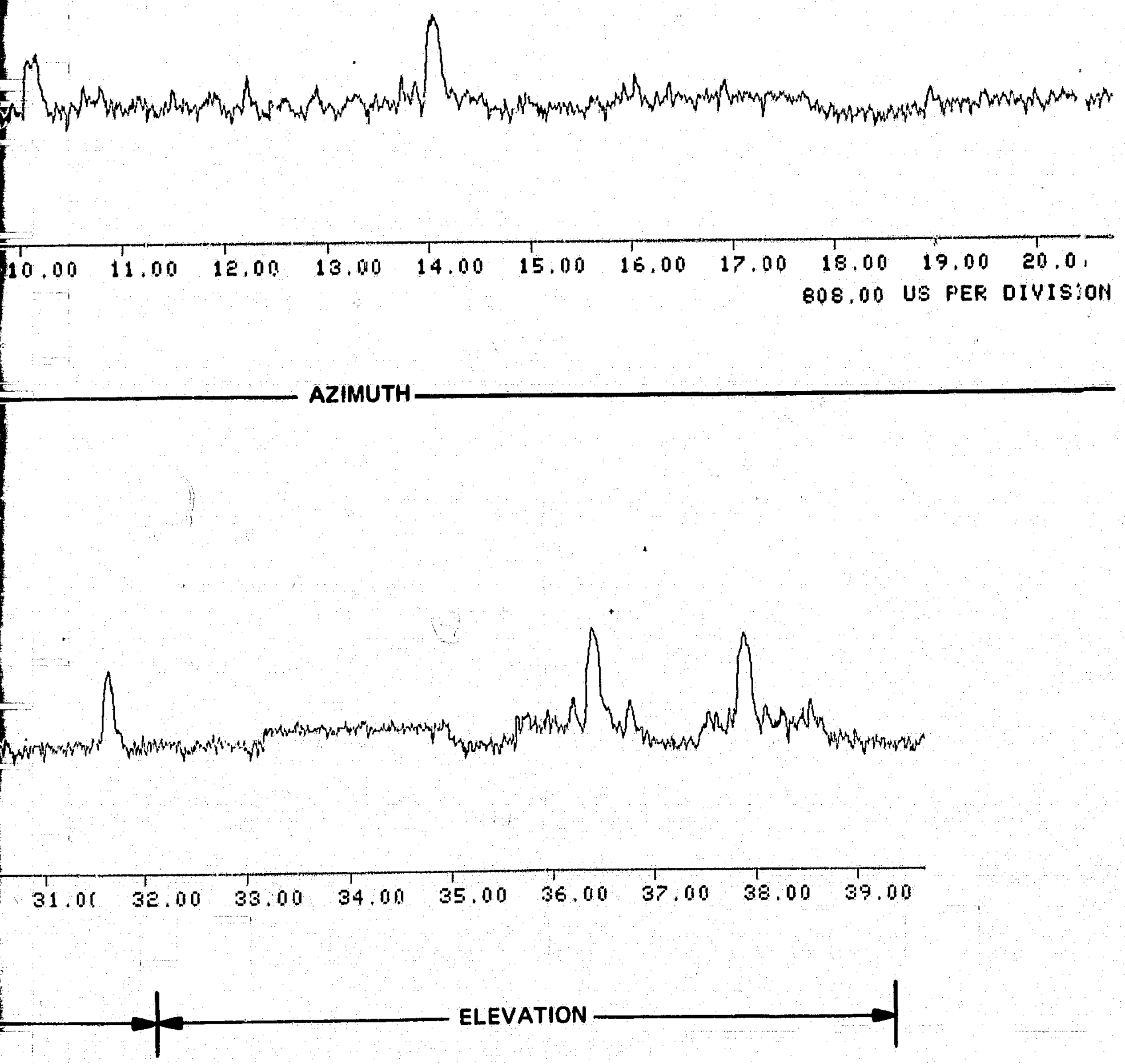
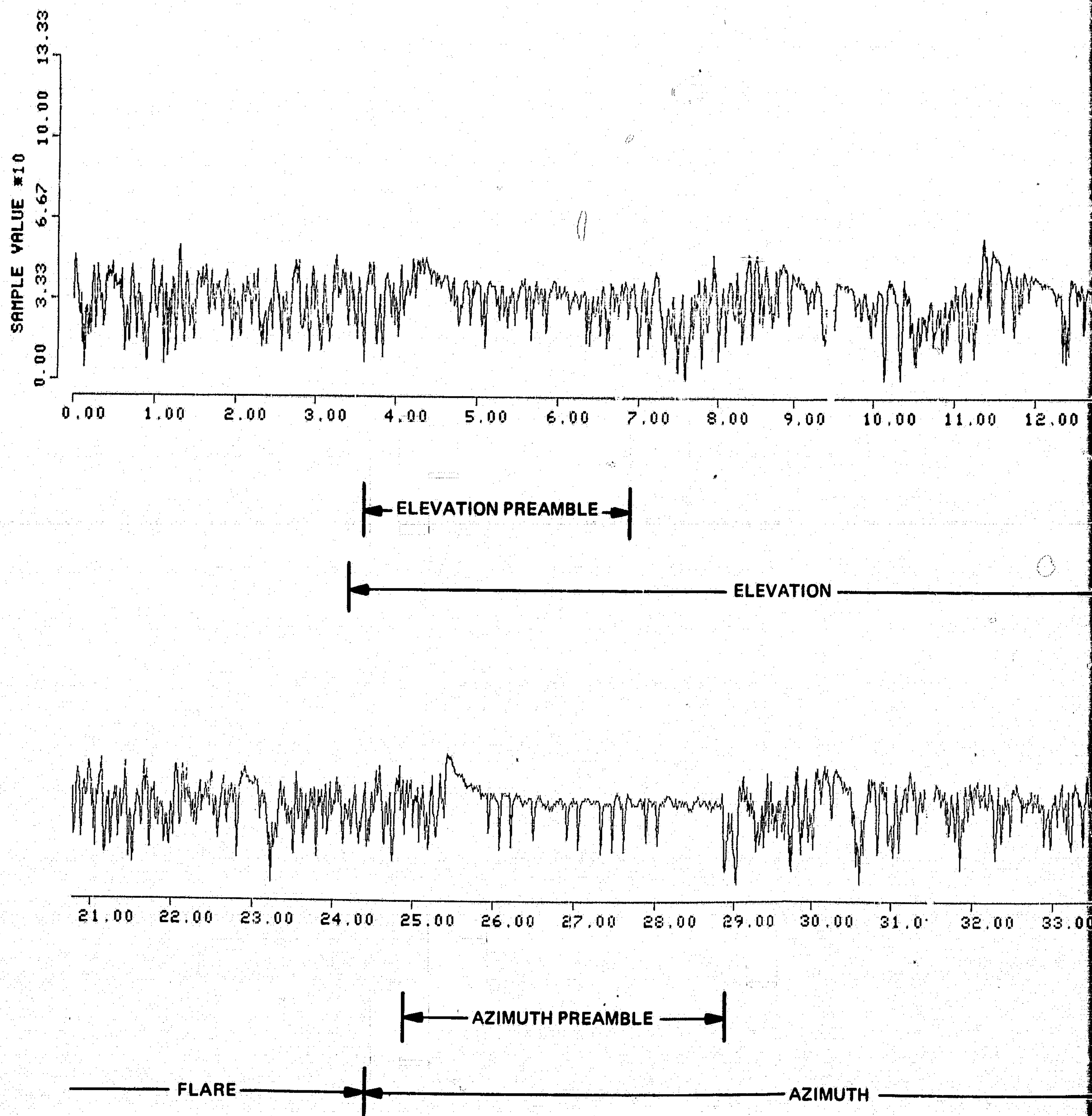


FIGURE 84. BENDIX BASIC WIDE LOG AMPLITUDE PLOT, 1 NM FROM RNWY 31, 6-23-78

FOLDOUT FRAME 2



FOLDOUT FRAME

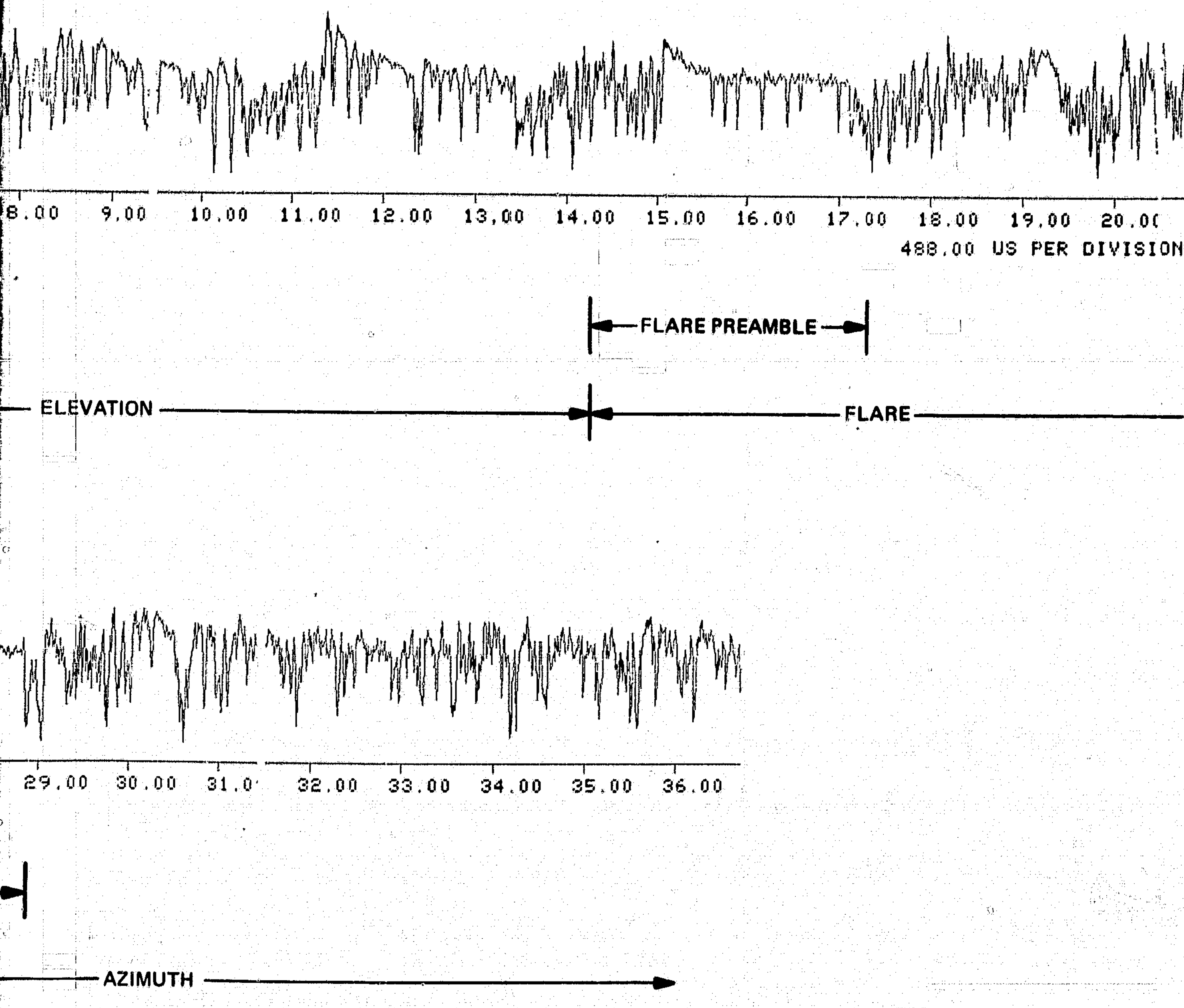
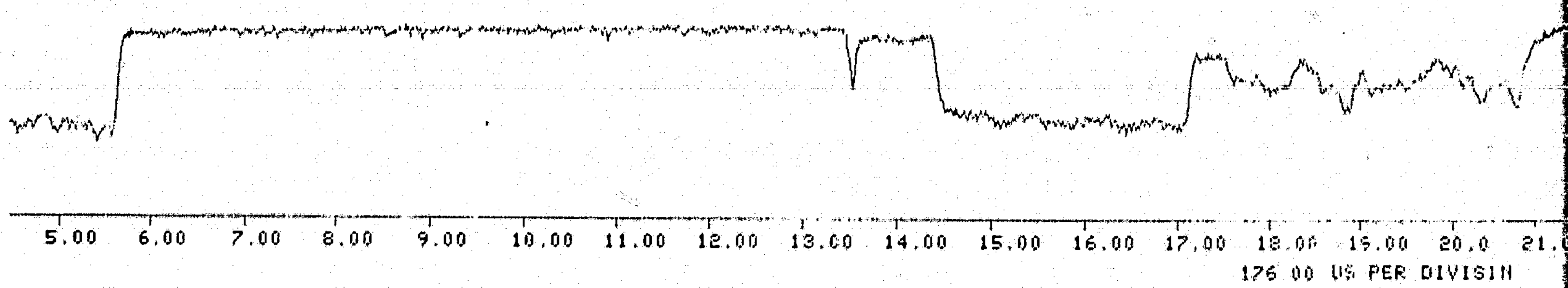


FIGURE 85. BENDIX BASIC WIDE DPSK PLOT,
1 NM FROM RNWY 31, 6-23-78

FOLDOUT FRAME 2


5.00
6.00
7.00
8.00
9.00
10.00
11.00
12.00
13.00
14.00
15.00
16.00
17.00
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20.0
176 00 US PER DIVISIN

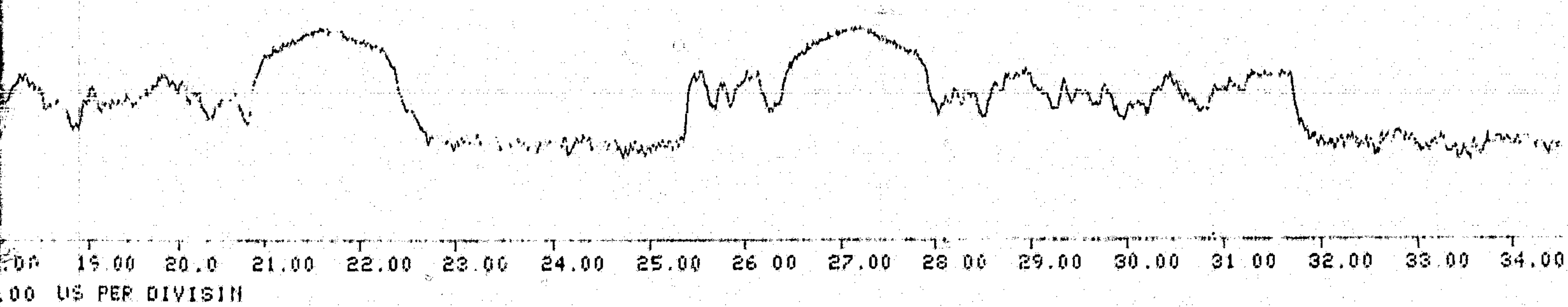
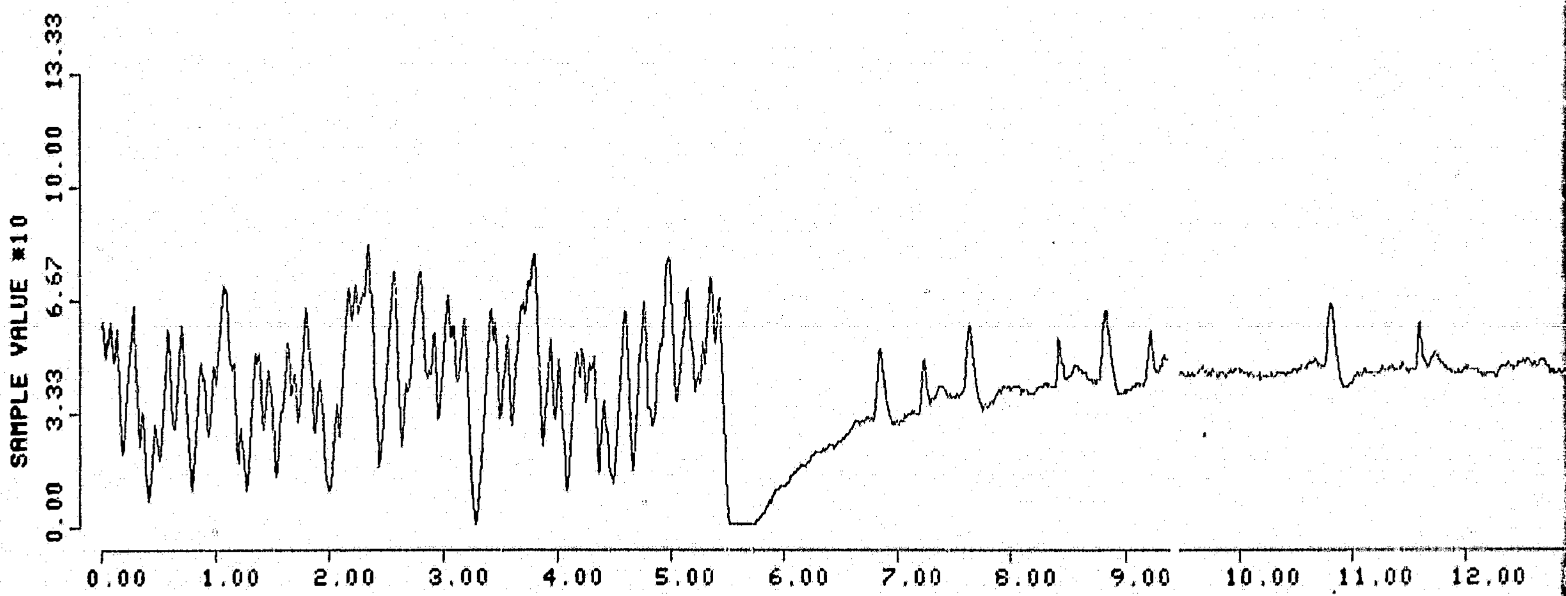


FIGURE 86. HAZELTINE SMALL COMMUNITY LOG AMPLITUDE PLOT, ELEVATION FUNCTION


SAMPLE VALUE *10
0.00
3.33
6.67
10.00
13.33
0.00 1.00 2.00 3.00 4.00 5.00 6.00 7.00 8.00 9.00 10.00 11.00 12.00

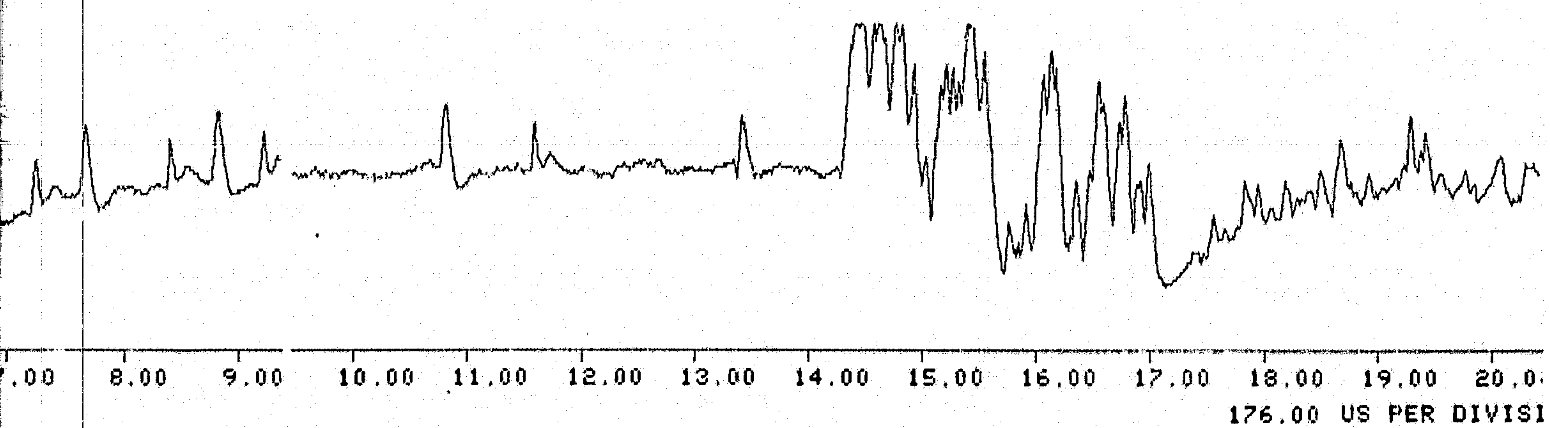


FIGURE 87. HAZELTINE SMALL COMMUNITY RECOVERED DPSK ELEVATION PREAMBLE

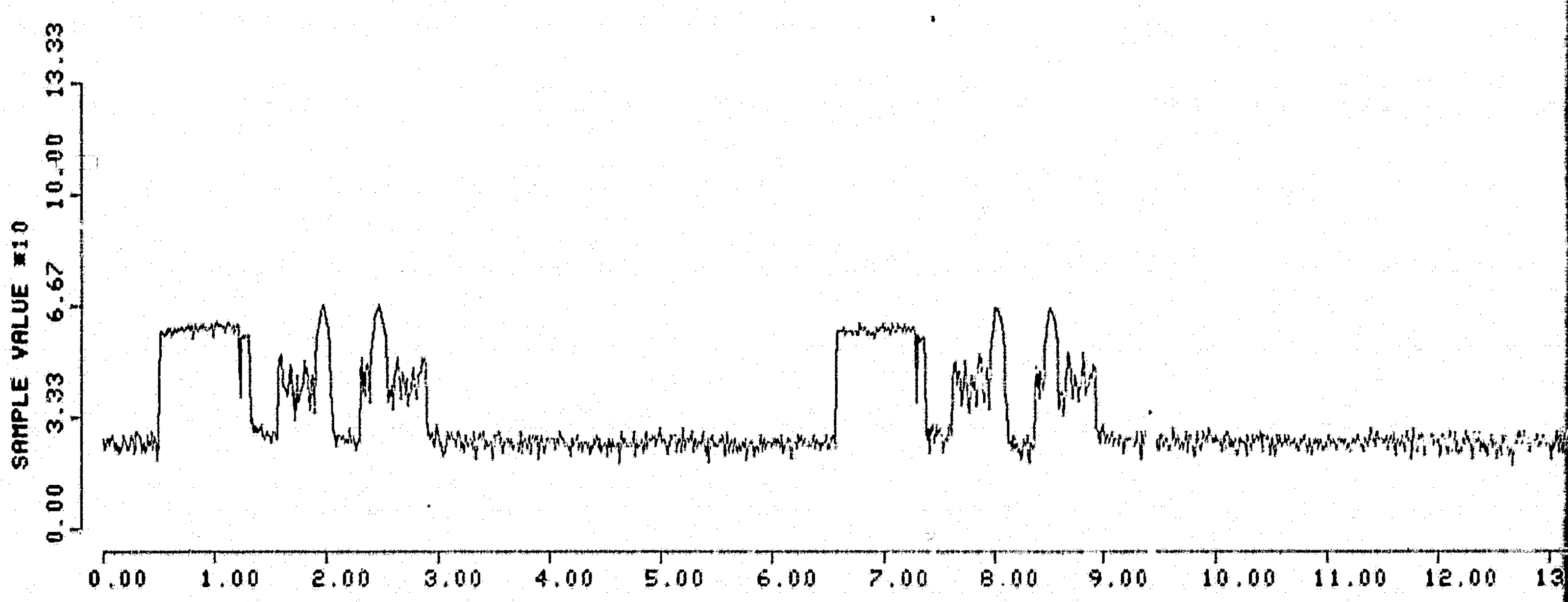
Figure 88 is a low resolution view of a random 73 msec period showing the repeated Elevation format.

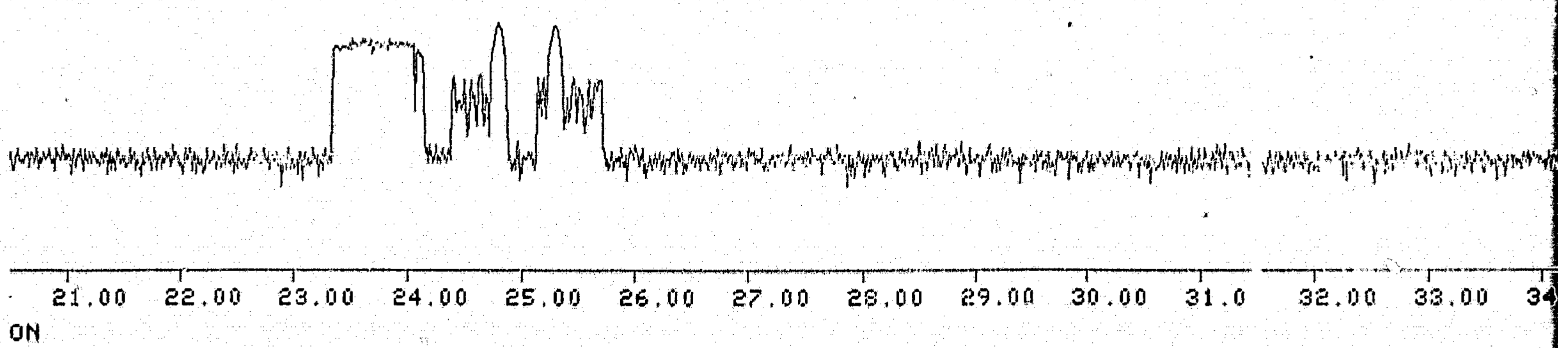
Figure 89 is the Azimuth format. The semi-hard switch DPSK is evident in the preamble. The Azimuth preamble shown in Figure 90 also shows the alternating amplitude detected phase transitions.

The LCMLS receiver did properly respond to the Elevation format and provide proportional guidance, however a large random meter movement was also present. The receiver did not properly respond to the Azimuth Signal. The signals are being further analyzed for clues to these behavior anamolies.

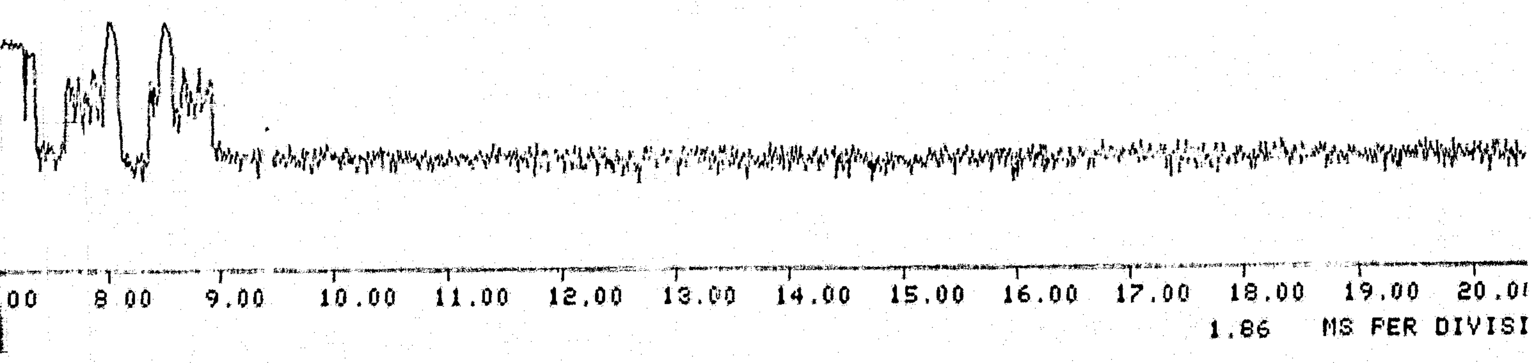
Summary of air/ground compatibility. - The LCMLS Receiver is compatible with all ground stations tested with the following provisions: 1) all ground systems must utilize a hardswtiched DPSK and 2) all ground systems must provide data words #1 and #2 for MLS ground system status.

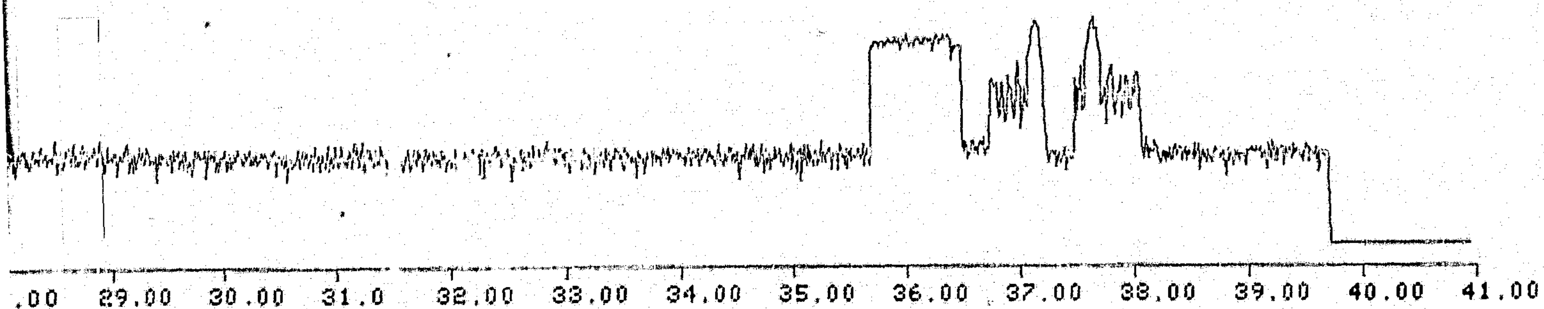
A potential compatibility problem presently exists for elevation sites which provide negative angle coverage of 1° or larger. For these sites, the elevation transmit time squeezes in very close to mid scan to a time region where the LCMLS receiver does not expect a carrier to be present. The result is a double set of "down" pulses and subsequent rejection of the data by the receiver. The solution can be implemented by significant modification of program firmware.





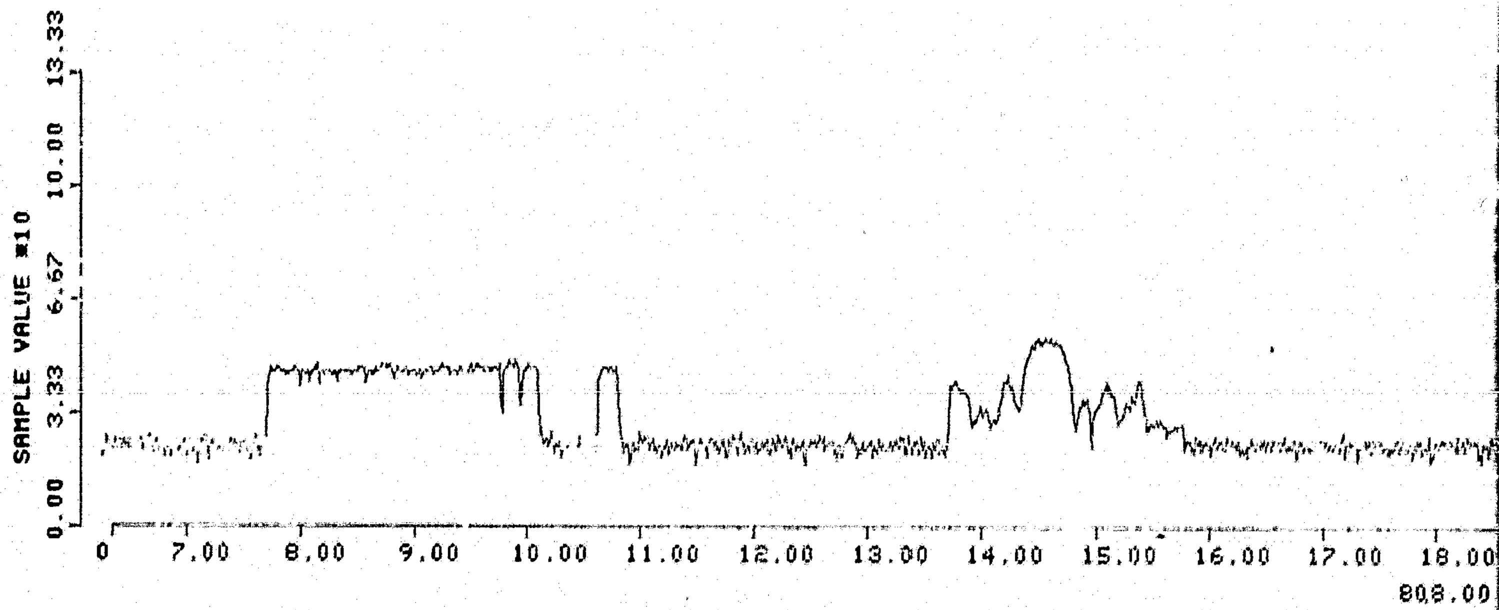
FOLDOUT FRAME





FOLDOUT FRAME 2

FIGURE 88. HAZELTINE SMALL COMMUNITY LOG AMPLITUDE ELEVATION FORMATS



ORIGINAL PAGE IS
OF POOR QUALITY

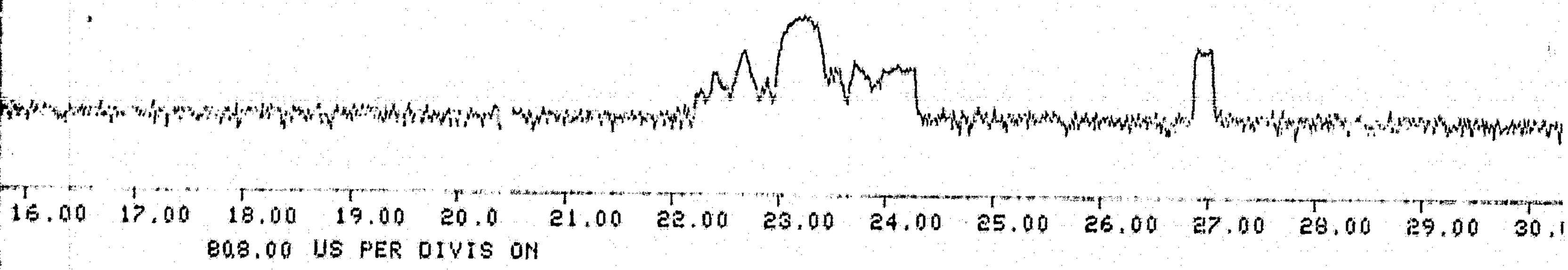


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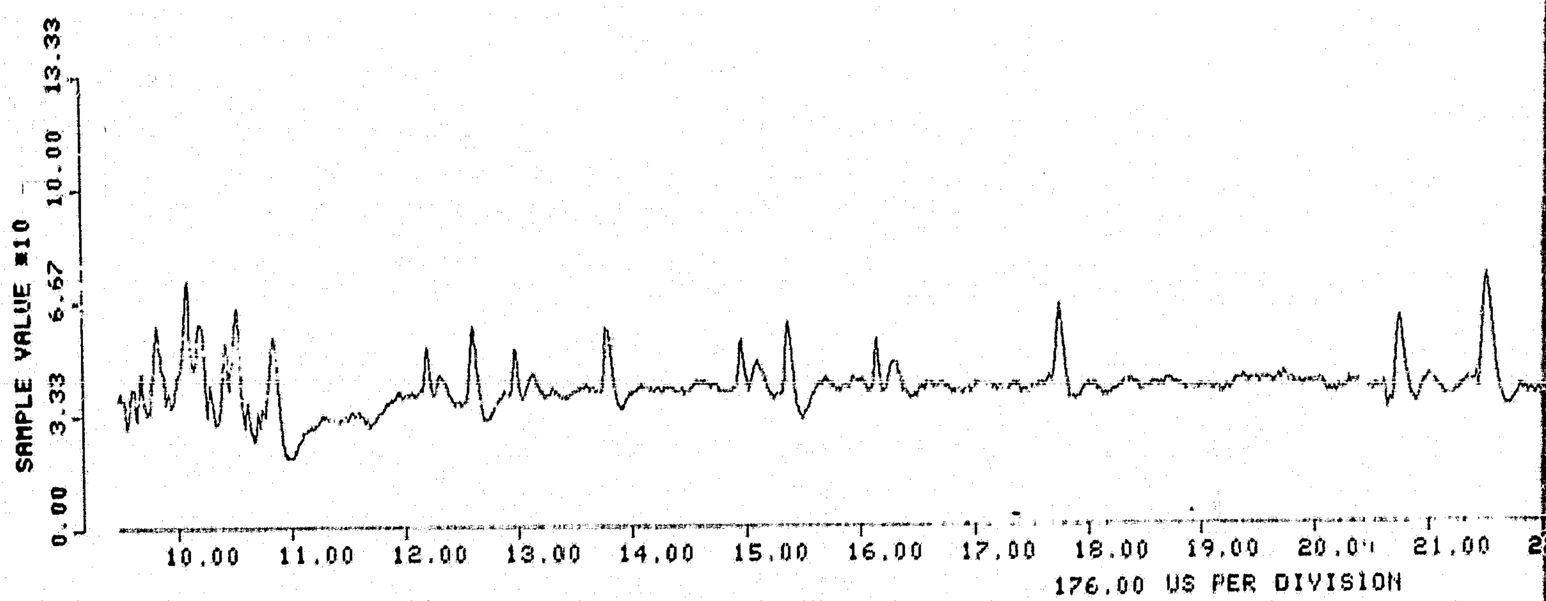
FIGURE 89. HAZELTINE SMALL COMMUNITY LOG AMPLITUDE AZIMUTH FUNCTION



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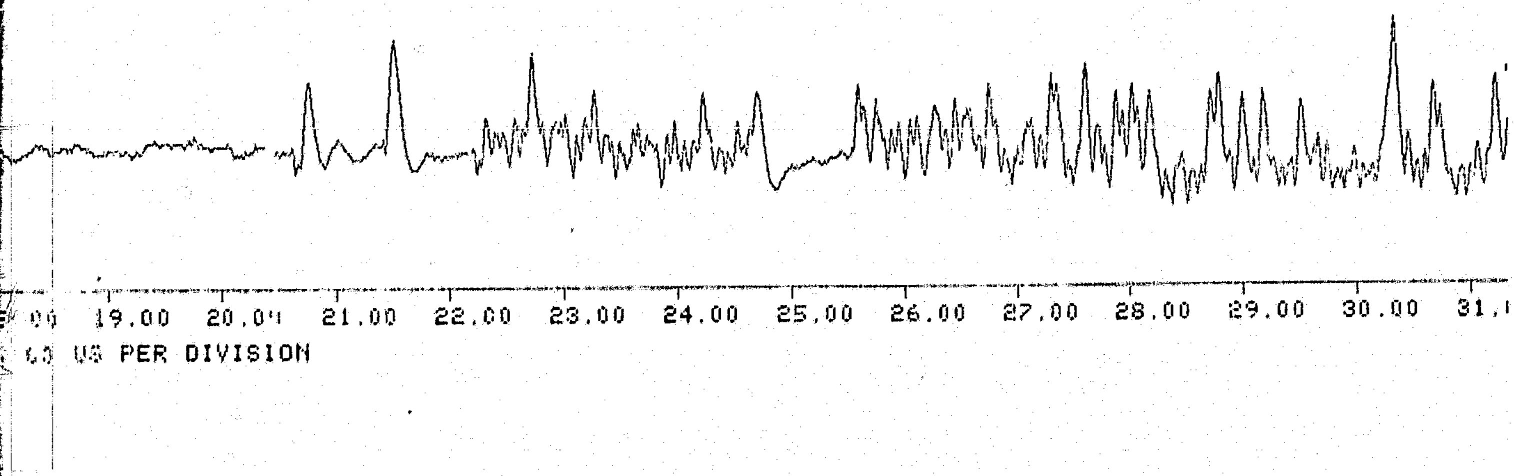

FOLDOUT FRAME 2

FIGURE 90. HAZELTINE SMALL COMMUNITY RECOVERED DPSK AZIMUTH PREAMBLE

PRODUCTION COST ANALYSIS

This section describes the production cost analysis of the developed MLS Receiver, in production lots of 2000. This cost analysis is intended for use as reference material only, and therefore it is necessary that any potential manufacturer contemplating entering this market be sure to substitute his particular methods and procedures for those presented herein.

Summary of Costs

Based on the configuration of operating prototype receivers (PRX's), the manufacturer's suggested sell price of the MLS receiver, with installation and warantees, is $1,486.54, or more likely rounded off to $1,485.00. This "bottom line price", is dependent upon several variables and is based on certain assumptions.

The variables are costs of material, parts, labor tooling, automation and quantity of production. The NASA Statement of Work dictated referencing all costs to a 1976 baseline; however, this became of dubious value due to the fact that labor costs have significantly increased while component costs have been mixed. For example, microprocessor and memory component costs have decreased, while certain microwave components have drastically increased. Accordingly, the $1,486 figure reflects 1978 material costs and 1976 labor rates.

The assumptions made in this cost analysis are of prime concern, because factory methods and conditions do vary significantly between manufacturers. The following section describes the assumptions made by AEL and NARCO.

Cost Analysis Assumptions

The cost calculations are based on the following assumptions:

1. The RF Head, being a sophisticated microwave assembly, would likely be purchased as a material item from a microwave oriented manufacturer, such as AEL, although several others exist. This microwave manufacturer would invest in tooling of the radome and stripline assemblies. The loadings for this microwave manufacturer would typically be 120% overhead and 70% G&A/profit. Therefore, if the MLS receiver manufacturer had the in-house capability of microwave assembly manufacturing, the RF head could be produced at a cost such as to effect a $32.40 material cost savings, and theoretically produce a receiver capable of selling below $1,375. It must be cautioned, however, that if this in-house microwave capability does not exist, there is likely significant risk associated with the development of this capability.

2. The factory assembly, inspection and test labor costs are $4.47, $4.91 and $5.74 per hour, respectively.

3. The factory manufacturing overhead is 200%. Items such as software support for automated test and lead insertion programs, engineering, etc. are included in this overhead. Sufficient detail of all printed wiring assemblies is included herein to allow a crosscheck of labor estimates.

4. The manufacturing assembly, inspection and test labor is estimated on a per-component basis of 0.015, 0.086 x 0.015 and 0.004 hours per component respectively. In addition, there is a 30 minute final test and set-up minimum. These factors are based on averages over several similar NARCO products, and include interassembly cabling, etc.

5. The mark-up factor, or gross margin, is 45%, calculated as follows:

$$GM = 1 - \frac{\text{DIRECT COST}}{\text{FACTORY NET}}$$

In other words, a 45% gross margin means that the ratio of factory net to direct cost is 1.818; therefore the avionics equipment manufacturer sells the receiver to a distributor for 1.818 times his direct cost, which covers all indirect costs such as marketing, advertising, return on investment, and also profit. A typical gross margin is 45%, with 40% expected in the early stage, 50% when the market appears to be prime, and eventually 40% as a mature market cut-off point.

6. The manufacturer's suggested list price, for an installed equipment, is exactly two times the factory net. This x2 multiplier is likely the most variable. The dealer/installer purchases the MLS receiver for $743.00; he "asks" $1,485.00 from the GA buyer. In the case of the AEL/NARCO developed MLS receiver, the typical installation costs are minimal, due to the use of flexible RG-58 cables, panel mounted receiver and top mounted RF head. It is expected that this MLS receiver unit will actually sell for as low as $1,250.00 each, with a typical sale being $1,400.00. The difference will primarily depend upon the particular aircraft installation, complexity of existing avionics, etc.

RF Head Cost Breakdown

The production cost estimate of the RF Head as manufactured by a microwave component corporation and sold to the avionics manufacturer is as follows:

Item	Subassembly Breakdown	Average Hourly Labor Rate	Man/Min	Labor Cost	Material Cost
1	Multiplier/Amplifier Assy.	4.10	30	2.05	10.46
2	Stripline Circuit Assy.	5.13	13.6	1.17	14.38
3	Metal Housing Fabrication	5.55	2.5	.23	.60
4	Radome Fabrication	4.46	0.5	.04	.20
5	RF Head Assembly	4.10	18.5	1.26	2.25
6	RF Head Test	5.13	30.0	2.57	-
7	Production Engineering	9.01	6.0	.90	-
			101.1	$ 8.22	$27.09

Total Labor Cost	8.22
Loaded Labor Cost	18.08 (120%)
Total Material Cost	27.09
Loaded Labor & Matl.	45.17
G&A & Profit	32.40
RF Head Producer Sell Price	$77.57

Receiver Cost Breakdown

The receiver cost breakdown, on a subassembly basis, is shown in Table 4. The cost loadings up through customer sell price is shown in Table 4.

TABLE 4. MLS REC. ASSEMBLY COST BREAKDOWN

Subassembly	No. of Parts	Component Price Quantity 2,000 (No. PC Boards)	(# Comp. x .015 Hrs/Comp Labor Hours Ass'y	Assembly Labor Cost
RF Head	1	77.57	0	
IF/Detectors	77	14.68	1.155	$ 5.16
Synthesizer	244	36.36	3.66	$16.36
Pre-Processor/ Processor	157	46.78	2.37	$10.59
Power Supply	48	17.12	.72	$ 3.22
Front Ass'y	17	5.62	.255	$ 1.14
Mechanical (incl. PC Bds)	---	44.86	---	
Installation	---		---	
Kit & Mtg Tray	---	(10.82)		
TOTALS	544	242.99	8.16 Hrs.	$36.47

TABLE 5. RECEIVER USER COST CALCULATIONS

Assy. Labor = $4.47/Hr x .015 hrs/Comp x 544 Comp =	$36.47
Insp. Labor = $4.91/Hr x 8.6% Assy. Hrs (8.16) =	3.45
Test Labor = $5.74/Hr x (0.5 Hrs +0.004 Hrs/Comp x 544 Comp) =	15.36
Total Labor	$55.28
Overhead @ 200%	110.56
Loaded Labor	$165.84
Elect. Material	198.14
Mech. Material	44.86
Total Material	$243.00
Total Direct Cost (LL&M)	408.84
Factory Net (45% GM)	743.27
Mfg Sugg List Price	$1486.54

Cost Comparison And Analysis

The estimated production cost appears to have progressively increased during the three tasks of the program. The following breakdown helps to examine the causes of the increases:

Item	Original Proposal	Task I Estimate	Task II Estimate	Task III Estimate
Number of Parts	413	311	429	544
Electrical Material Cost	$ 158.26	$ 190.18	$ 174.34	$ 198.14
Mechanical Material Cost	$ 51.91	$ 38.38	$ 38.38	$ 44.86
Direct Labor Cost	$ 51.91	$ 40.13	$ 53.37	$ 55.28
Total LL&M	$ 355.48	$ 348.95	$ 372.83	$ 408.84
Customer Sell Price	$1235.00	$1269.00	$1356.00	$1486.54

Tooling costs, RF head. - Tooling costs for the various operations associated with volume production of the RF head are itemized below:

1.	Punch & Drill of Printed Circuits	$ 4,900
2.	Photo etching Tooling	700
3.	Contour Punching and Stripling	4,100
4.	Tooling for Plated Thru Holes	600
5.	Randome	4,500
6.	Bottom Enclosure	200
7.	Assembly aids	1,650
	This tooling represents loaded labor and materials	$17,650

Again, this tooling cost estimate is a function of the technology and methodology base of the microwave component manufacturer involved.

Tooling cost, panel mounted unit. - The following list shows estimated tooling costs for the panel mounted unit:

Description	Tooling
Top & Bottom Covers	200.
Side Panels	000.
Heat Sink, Rear, Extrusion	725.
/ Trim Panel, Die Cast	6,600.
Base Plate	55.
Dial, Frequency	3,500.
Cam for Micro Switch	2,000.
Dial, Glide Slope Switch	2,100.
Dial, 0-1	2,000.
Knob, Freq. Select	
Knob, Bar, FM Chan., Glide Slope	3,000.
Lens, Channel Select	1,000.

(continued on following page)

Description	Tooling
Lens, Warning	1,000.
Light Shield, Channel Select	1,500.
Switch Board, 3 Switches	800.
Total	$ 25,380.

Tooling cost would be a necessary investment for any avionics equipment manufacturer entering the MLS receiver market. This cost will vary significantly from manufacturer to manufacturer, dependent upon pcakaging and use of hardware existing on standard product lines.

Conclusions Of Cost Analysis

The cost analysis increased by about 20 percent during the program, due to the updates in the design as the equipment entered breadboard, brassboard, prototype stages and onto bench testing and actual interface to the ground MLS transmitters. The major portion of this growth is due to labor rate increases from 1976 to 1978.

Nevertheless, the design described within this report represents the simplest, most straightforward technology known by AEL and NARCO. As technology upgrades, likely the synthesizer circuitry may become simplified; it is not forecasted that the other areas of the MLS receiver will become simpler within the near future of 5 to 10 years.

What may become feasible, however, is to be able to add functions and features without significantly increasing the unit cost. This improvement would be a direct result of technological advances in microprocessors, D to A converters, memory circuits, etc., within the above mentioned time frame.

PREFLIGHT TEST UNIT

For the purposes of both bench and flight line testing, a Preflight Test Unit (PTU) was constructed by AEL using several components common to the prototype receiver. As a result, a 200 channel synthesized PTM was readily achievable. The capabilities that the PTU was designed to meet are listed below in Table 6.

TABLE 6. PREFLIGHT TEST UNIT CAPABILITIES

Function	Description
1. RF Output	200 channels, switch selectable, C-Band -45 dBm to -105 dBm continuously variable. Power set adjustment ± 6 dB. Frequency stability ± 50 kHz. Fixed frequency outputs at 10.8 MHz and 160.8 MHz.
2. Az Function Modulation	Fixed DPSK Barker Code, Function I.D., Facility I.D.
	Selectable Guidance Pulses
	Selectable SLS Pulses (right, left, rear) and Variable Amplitude +2 and -8 dB relative to "TO-FRO" Pulse Amplitude
	Variable "TO-FRO" Pulse Spacing Corresponding to 39.9°.
	15 Selectable "TO-FRO" Pulse Widths From 20 μsec to 300 μsec in 20 μsec steps
	Fixed "TO-FRO" Test Pulse
3. El Function Modulation	Fixed DPSK Barker Code and Function I.D. Switch Selectable Minimum Selectable Glidescope From 2.0° to 16.0° (32 Selec.)
	Selectable SLS Pulse With Variable Amplitude +2 and -8 dB Relative to "TO-FRO" Pulse
	Variable "TO-FRO" Pulse Spacing Corresponding to -2° to +29.9°.
	15 Selectable "TO-FRO" Pulse Widths From 20 μsec to 300 μsec in 20 μsec steps.

TABLE 5. PREFLIGHT TEST UNIT CAPABILITIES - CONTINUED

Function	Description
4. MLS Ground Status	Variable Azimuth and Elevation Ground System Status Provided Via Basic Data Words #1 and #2
5. Angle Displays	Separate 4 Digit Azimuth and Elevation Displays, Resolution to 0.1°, Accuracy Typically ± 0.05°.
6. Propeller Modulation	Continuously Variable Amplitude Over 0 to 12 dB Modulation Depth and Continuously Variable Frequency Over 30 to 200 Hz.
7. Auxiliary Outputs	DPSK Data DPSK Data Clock Guidance, SLS, TO-FRO Pulses Scope Trigger(s) Prop. Mod. Output @ Fixed Level
8. Input Power	120 VAC 40-400 Hz 1ϕ or 14/28 VDC
9. Service Conditions	-15°C to +55°C - 95% Humidity - No condensation

Detailed Description of PTU

The frequency selection provides a fixed level output of any one of 200 synthesized channels with amplitude variable from -45 dBm to 105 dBm. In addition, a power set adjustment of ± 6 dB is provided as a calibration aid. Two fixed frequency outputs of 10.8 MHz and 160.8 MHz are made available as test aids.

The aximuth function "TO-FRO" pulse width is any one of 15 selectable pulse widths from 20 μsec to 300 μsec in 20 μsec intervals. Increasing the pulse width range beyond the previous 25 and 250 μsec allows a go/no-go test of the PRX pulse width discriminator.

The minimum selectable glideslope is selectable from 2.0° to 16.0° in 32 increments as defined in the modifications to ER-700-08A, and discussed at NASA Ames on 3/29/77.

The elevation angle "TO-FRO" pulse spacing coverage is selectable from -2° to +29.9° as defined in the modifications to ER-700-08A.

As a test aid, the propeller modulation signal is provided at a fixed level for test oscilloscope synchronization.

PTU Block Diagram Description

The block diagram of the PTU is shown in Figure 91. The RF chain begins with a 10.8 MHz source which is a phase locked loop referenced to the synthesizer 4.8 MHz crystal oscillator. The combined stability of the 10.8 MHz source and the synthesizer insure a "C" band output within ± 50 kHz of the desired frequency. A variable attenuator with 60 dB of range is incorporated at the 10.8 MHz IF to eliminate the large size, cost, and tedium of a 5 GHz unit. The DPSK modulator is a passive double balanced mixer and the amplitude modulator is a linear, active element.

A 150 MHz source in the synthesizer is used to up-convert the 10.8 MHz in a passive mixer to 160.8 MHz where the composite signal is filtered in a bandpass filter identical to that used in the PRX 1st IF. The 160.8 MHz IF is then up-converted to the desired 5 GHz MLS operating frequency by using the Low Cost MLS receiver microwave front end stripline assembly operating in reverse.

The 200 channel synthesizer is identical to that of the prototype MLS Receiver.

Three RF outputs are provided as test aids for the LCMLS receiver. Each output is a variable amplitude composite signal which can drive the PRX at the 2nd IF of 10.8 MHz, the first IF at 160.8 MHz, or the "C" band operating frequencies of 5031 to 5090 MHz.

PTU Modulation

The sequence generator provides proper timing and enabling signals to the DPSK data registers and the "TO-FRO pulse" generators such that the master and sub-sequence formats are generated. The master sequence is identical to the ER-700-08A specification. Basic Data Word #2 has been placed between the first sub-sequence #2 and the second sub-sequence #1. This placement is arbitrary; however, it meets the ER-700-08A guideline for placement within a jitter period.

The DPSK Data Register are labeled AZ DPSK, EL DPSK, Data Word 1 and Data Word 2. In simplified form they are parallel in-serial out devices accepting hardwired inputs such as the Barker Code, function I.D., etc., and front panel inputs such as EL Status, AZ Status, Min. Glideslope, etc. As the data is strobed out of the registers, it is encoded with a 15 kHz clock to form the proper ER-700-08A DPSK format. In addition to data formatting, these registers also output a reference time to enable the "TO-FRO" pulse generators.

The "TO-FRO" pulse generators for AZ and EL are identical in form with the AZ generator providing several additional pulses such as L-R guidance, left-right-back SLS pulses and "TO-FRO" test pulses. In addition to generating the precise timing for the "TO-FRO" pulses, circuitry is included for setting the precise width

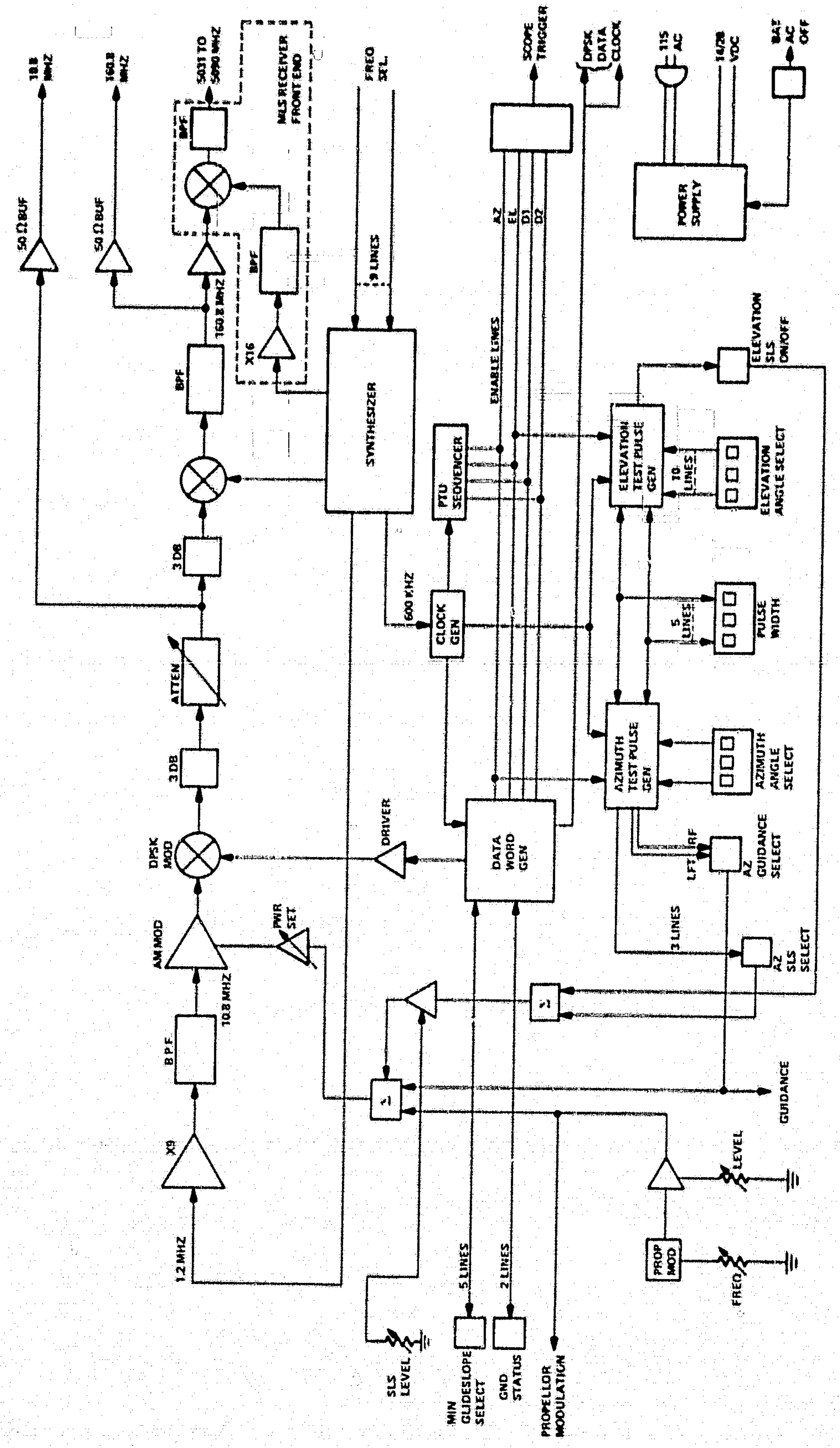

FIGURE 91. PREFLIGHT TEST SET BLOCK DIAGRAM

of the "TO-FRO" pulses and cross coupling pulse width information with timing such that perfect centroid symmetry about mid-scan is maintained for all conditions of pulse width and selected angle.

PTU Packaging

The PTU is packaged in a single box shown in Figure 92.

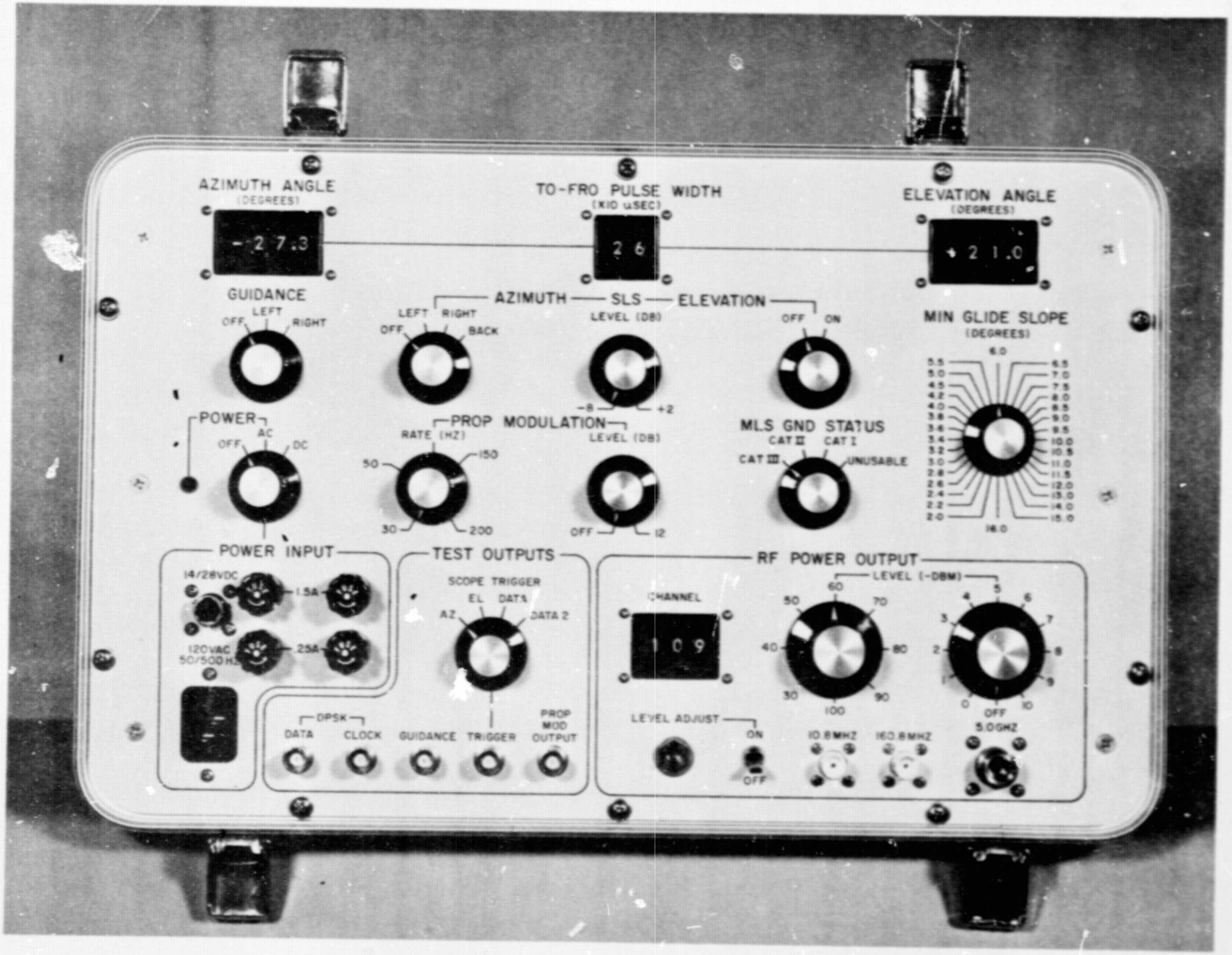

FIGURE 92. PREFLIGHT TEST UNIT FRONT PANEL

RECOMMENDED IMPROVEMENTS TO THE MLS RECEIVER

As a result of testing of the two prototype MLS receivers, it has become apparent that certain shortcomings of the equipment exist, which are hereby recommended as future improvements.

RF Head Improvements

The single stage transistor IF amplifier within the RF head does not perform adequately over temperature. This stage must provide about 15 dB of gain at 160.8 MHz; however, due to the varying mixer diode impedance at the amplifier source and the potentially varying load due to the length of coax between the RF head and the panel mounted unit, this amount of gain is overly optimistic and connot be achieved in a stable manner over temperature extremes, resulting in degradation of receiver sensitivity.

It is recommended that the RF Head design be modified to utilize either an improved single or a two stage amplifier with impedance buffering at the output.

Panel Mounted Unit Improvements

A shortcoming of the receiver within the panel mounted unit is that the sensitivity is not optimized and is not constant over temperature. This is caused by gain and limiting level variations within the CA3089 IC. Again, as in the RF head, the gain ahead of the CA3089 is marginal over temperature. The improvement discussed above for the RF Head will tend to improve this situation; however, more gain ahead of the CA3089 is also necessary within the panel mounted unit itself.

The CA3089 performs both the DPSK detection and the log IF detection, within a common predetection bandwidth of about 225 kHz. More DPSK sensitivity could be achieved by use of a phase lock loop detector with a 30 kHz effective tracking bandwidth. This change alone could effect as much as an 8 dB increase in DPSK sensitivity. A simple PLL circuit is now allowable since hard switching of the ground transmitter appears practical. Several low cost PLL's are available.

<u>Receiver added features.</u> - It is desirable to add the features of 1) selectable azimuth, 2) wide angle coverage, 3) higher azimuth updates, and 4) data interface per ARINC 582 format.

The selectable azimuth function would permit the pilot to select approaches to perhaps ± 40° in 5° increments.

The wide angle coverage would allow pilot selection of displayed azimuth angle range to ± 60° max.

The high azimuth update function would provide the capability of up to 40 updates per second.

ANTENNA PLACEMENT STUDIES

It is recommended that the optimum RF Head antenna placements be determined for several generic aircraft types. This antenna pattern data would prove necessary in order to firmly establish installation procedures and costs.

AUTOMATIC ANTENNA SWITCHING

The present low cost MLS concept utilizes a single forward looking RF Head/ Antenna. On certain aircraft, it may be necessary to utilize two RF Heads in order to obtain the desired coverage. In this event, an automatic antenna switchover technique must be used. The simplest technique is to alternate the heads at a fixed rate and require the processor to pick the signal with the largest amplitude. Other more sophisticated techniques, which do not half the information received, are also achievable.

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